Multi-channel Testing Architecture for High-speed Eye-diagram Using Pin Electronics and Subsampling Monobit Reconstruction Algorithms

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Abstract— **This paper proposes a new multi-channel testing architecture for high-speed eye-diagram. The proposed architecture reconstructs the eye-diagram of a multi-Gbps bit pattern with the combination of pin electronics and reconstruction algorithms. A scalability of the test system significantly increases in behalf of a monobit receiver and its designated reconstruction algorithm. A novel reconstruction algorithm using monobit receiver and subsampling clock enables the test system to monitor the signal quality in low-cost. The proposed architecture is implemented and demonstrated in a hardware prototype. Experiment with the hardware prototype shows that an eye-diagram of 3.2Gbps bit pattern can be reconstructed within sub-picosecond resolution by the proposed method with subsampling clock (below 100MHz).**

Index Terms— **Monobit receiver, Eye-diagram, Pin Electronic, High-speed Bit pattern.**

I. Introduction

MULTI-CHANNEL multi-Gbps digital I/O test systems are required to be equipped with channel monitoring capability to detect any failure or signal quality degradation while testing is being conducted. The potential channel failure includes connector wear-out, probe misalignment and the performance degradation of the device I/O. However, multi-channel pin electronics devices that are compatible with high-speed signaling and also equipped with channel monitoring functions are not readily available for tester development [1]. Cutting-edge field programmable gate arrays (FPGAs), which are widely used for the development of digital testers, are equipped with channel (or eye-opening) monitoring capability on their high-speed transceiver ports. However, the transceiver interface is not designed to be used as pin electronics. It is usually limited by its input dynamic range or dedicated to a particular type of signaling (i.e. differential signaling).

There are efforts to develop multi-Gbps PE (and eye-opening monitoring) chips. In [2], 8Gbps CMOS-PE macro was developed, which can be used for developing multi-channel test systems with eye-opening monitoring capability. In [3, 4], high-precision eye-opening monitor (EOM) circuit and adaptive control scheme were developed. The combination of high-precision EOM and adaptive decision-point control scheme improves the receiver sensitivity [3]. In [4], a 10-Gbps adaptive look-ahead decision feedback equalizer (LADFE) is used to measure eye-diagram and fabricated in 90-nm CMOS technology. However, in commercial area, pin electronics chips that can be purchased are mostly low-speed so not compatible with the frequency required for the cutting-edge digital device testing [5]. Tester design companies provide their own multi-channel high-speed pin electronics components and associated test systems, but such components may not be available for engineers and researchers outside their research collaboration. For this reason, the development of low-cost multi-Gbps digital I/O test and measurement systems with advanced features such as eye-opening monitoring and channel characterization is needed.

We propose an FPGA-based multi-channel digital I/O test system with PE modules equipped with eye-opening monitoring capability using off-the-shelf components to reduce the overall development and test cost. 16 PE modules can be mounted on the test system, and the I/O of each module is connected to the high-speed transceiver of a back-end FPGA controller to enable multi-Gbps signaling. The PE module contains off-the-shelf components such as drivers, comparators, level-setting DACs and power splitters. In addition, a pattern/timing generator can be implemented with additional hardware and logics in the FPGA, but it is not part of this research.

The overall architecture of the proposed method is presented in Section II. The detailed signal reconstruction algorithm is described in Section III. The optimal choice of the sampling frequency and the frequency of threshold signal is studied in Section IV. In Section V, hardware measurements with a FPGA board and a clock-comparator show the results of the reconstruction.

II. Approach

Fig.1 shows the proposed multi-channel testing architecture. The FPGA not only performs a transceiver but also provides a

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sampling clock for the clocked comparators and controls the DAC. The FPGA creates a multi-Gbps bit pattern through its high-speed IOs that dedicates to transmit a high-speed digital signal with the programmable logic resources. The high-speed bit pattern is re-transmitted by the driver that is a high-speed, low-jitter buffer with a programmable output swing and a programmable pre-emphasis. The DUT is stimulated by the high-speed bit pattern and the response signal is captured by the monobit receiver. The input response signal is subsampled and compared with the voltage level of the DAC that is controlled by the FPGA logic and synchronized with the subsampled clock signal.

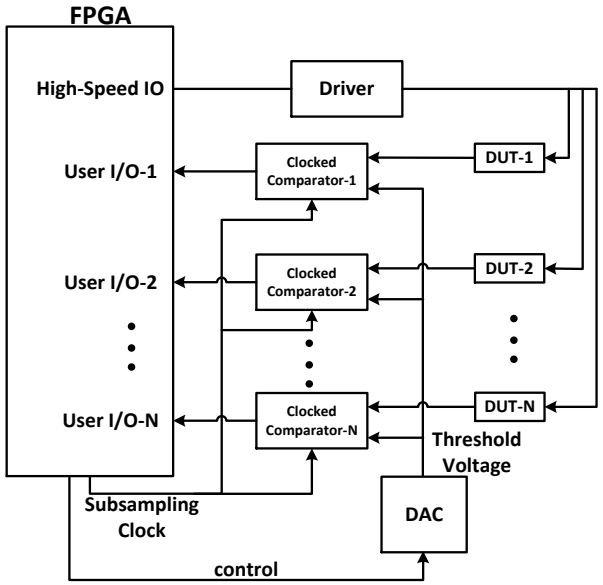
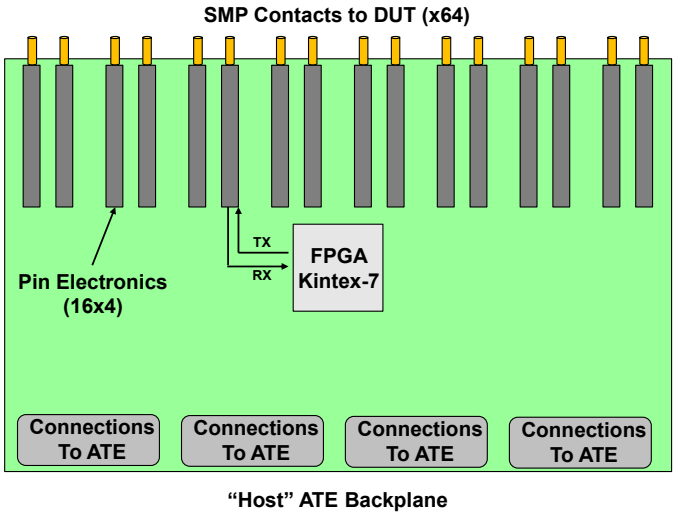


Fig. 1. Block diagram of the proposed multi-channel testing system.

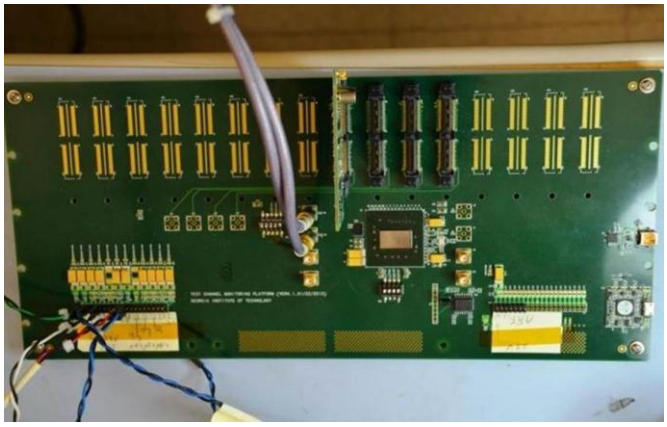
One of the key contribution of this work is the high-speed input signal is reconstructed by the monobit receiver with very fine time and amplitude resolution using subsampling clock and a low-cost DAC. This feature enables the test architecture to have high-scalability because the hardware resource for a channel is minimized. The detail electronic features of the proposed architecture will be discussed in the next section.

III. FPGA TEST SYSTEM HARDWARE AND PIN ELECTRONICS

A block diagram for the prototype test system is shown in Fig. 2(a) and a photograph is shown in Fig. 2(b). The test system is constructed on a printed circuit board that fits within the test head of a commercial ATE, taking up two of its standard expansion slots. On the bottom of the card are several multi-pin connectors that support communication buses and obtain power through the "host" ATE backplane. Central to the design is a Xilinx "Kintex-7" 28nm CMOS FPGA that serves as a local test controller for the card. The FPGA receives test pattern data, test control parameters, and high-level commands from the host ATE. Otherwise, the FPGA performs the desired tests autonomously, without real-time interaction with the host ATE. Essentially the FPGA is programmed to act as a stand-alone local tester. High-speed signals are generated and received by Xilinx "GTX" multi-Gigabit transceiver logic. The particular FPGA used in the prototype has 16 TX and 16 RX fully-differential ports, each capable of supporting signals up to 13Gbps.



(a)



(b)

Fig. 2. FPGA-based test system on a printed circuit board, (a) block diagram and (b) photograph of the prototype PCB.

While the FPGA is very good at generating and receiving multi-Gbps serial test patterns, it has limited ability to vary the test signal analog characteristics, such as voltage amplitude, offset, time-delay, signal pre-emphasis, etc. Therefore, to complement the FPGA and provide a wider range of signal variation, "pin electronics" (PE) modules are added to the signal paths. For the prototype, a PE module was designed that includes all the electronics for four bidirectional multi-Gbps signals. Multi-pin connectors are arranged near the top edge of the PCB for attaching 16 of these PE modules, for a total of 64 channels. During the development phase only four of the 16 PE modules were actually populated on the prototype PCB. Nevertheless, all 16 positions are shown to illustrate the feasibility of scaling up to the full 64-channel test system. In the photograph (Fig. 2(b)) the four active PE card connectors are visible just above the FPGA with a single PE card actually present in one of them.

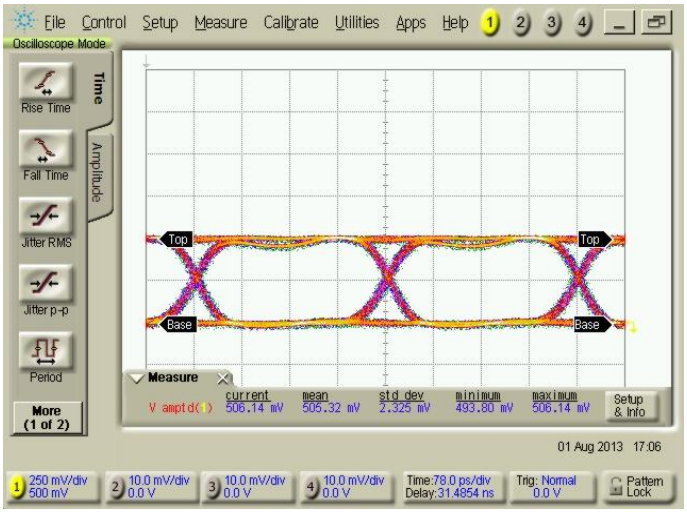
The patent-pending design of the PE module includes signal drivers (Tx), receivers (Rx), samplers, signal conditioners,

programmable delay elements, serial DACs, relays (for connecting to the host ATE parametric measurement units and low-speed test electronics), and high-bandwidth connectors (for passing the signals between the module and the FPGA and the DUT). Using only off-the-shelf components, the 4-channel PE module is able to accurately produce and measure signals up to 5 Gbps. Other performance characteristics are listed in Table I.

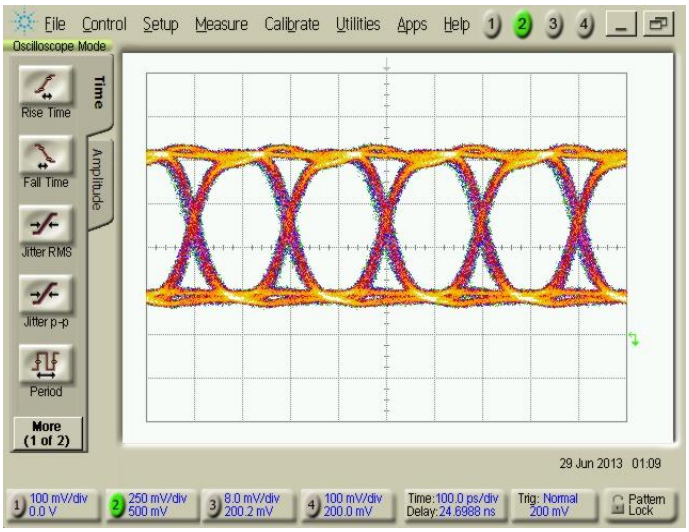
TABLE I. 4-CHANNEL PE MODULE PERFORMANCE CHARACTERISTICS

Number of channels	4
Maximum data rate (DNRZ)	5.0 Gbps
Driver rise-time (20-80%)	45ps (typical)
Driver amplitude range	100mV to 1000mV (single-ended)
Driver DC offset range	-0.2V to +1.2V
Driver Pre-emphasis control	5-bit digital, including amplitude and duration
Comparator input sensitivity	<10mV (typically <5mV)
Comparator range	0V to 2.5V
Delay Resolution (lsb)	5ps
Delay Range	5000ps (5ns)
Random Jitter	1ps (typical, limited by reference clock jitter)
Deterministic Jitter	<5ps
Transmission line bandwidth	>5GHz

To illustrate the pin electronics driver characteristics, a multi-gigabit-per-second serial data pattern is generated by the FPGA GTX circuitry and passed to a PE module. After adjusting its delay and voltage characteristics the resulting data "eye" diagrams are shown in Fig.3, using an Agilent 81600D sampling oscilloscope with a 50 GHz bandwidth sampling head. The top figure (Fig. 3(a)) shows the signal at 3.2Gbps, and Fig. 3(b) shows it at 5.0Gbps. In each case, the pre-emphasis characteristics (duration and amplitude) of the drive signal are adjusted in order to obtain the optimal eye shape at the receiving end of the transmission line (at the oscilloscope input in this case). The pin electronics channels support multiple receiver/sampler circuits that support characterization tests in parallel with functional testing. This allows the driver and DUT signals to be checked while running normal functional tests as well as during offline testing (for set-up, calibration, and signal optimization).



(a)



(b)

Fig. 3. Pin electronics (PE) card driver output data eyes, (a) 3.2Gbps at 78ps/div, (b) 5.0 Gbps at 100ps/div.

IV. EYE RECONSTRUCTION ALGORITHM BY MONOBIT-RECEIVER

A. Sampling Time-location: Synchronized Fractional Subsampling

In [prior work of eye-monitoring], the synchronized sampling clock is time-delayed to sample the different parts of the signal within the bit-period. However, the quality and the time-resolution of the reconstruction are limited by the accuracy of the delay IC. In this paper, the synchronized fractional subsampling is proposed. A fine time-resolution of the reconstruction is achieved by the frequency offset between the sampling clock and the input signal. The time-resolution can be configurable by changing the fractional relationship.

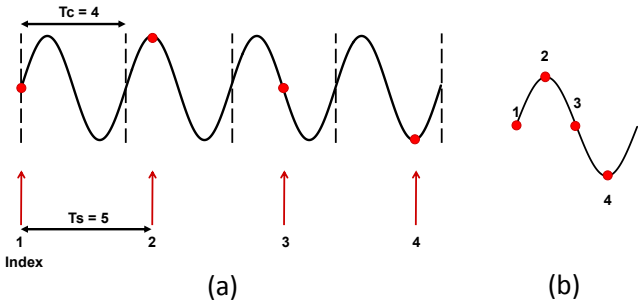


Fig. 4. (a) Synchronized fractional subsampling, and (b) its reconstructed waveform.

In Fig. 4(a), one example of the synchronized fractional subsampling is shown. In this example, the bit-period of the input signal and the period of the subsampling clock has 4/5 relationship. As the input signal and the sampling clock are synchronized, the phase between them is not drifting over the time. Moreover, the phase changes with a period of 4 due to the fractional relationship. Therefore, the synchronization and the fractional relationship create periodic phase offset over the time.

In general, when the frequency relationship between the sampling clock (f_s) and the input signal (f_c) is as following,

$$f_s = \frac{C}{D} f_c$$

where C and D are coprime, then C is the number of the sampling time-location. Thus, the time-resolution of the reconstruction is configurable by changing the frequency relationship. We refer D as the subsampling factor. It is also notable that there are infinitely many choices for the frequency of the sampling clock with a given desired time-resolution because D is independent with the resolution. In Fig. 4(b), the samples over the period are gathered and the signal is reconstructed by plotting the samples in proper index order.

B. Monobit Eye-reconstruction: Logic Distribution

In this proposed testing system, a monobit clocked-comparator performs as the monobit receiver. The monobit clocked-comparator compares the input signal and the threshold voltage level at the rising edge of the sampling clock. If the input signal is higher than the threshold at the clock edge, the clocked-comparator outputs a logic one. Otherwise, the output is a logic zero.

The reconstruction of the eye-diagram is achieved by adjusting the sampling point and accumulating the output logics from the clocked-comparator. The sampling location can be configured by the combination of the synchronized fractional subsampling and the programmable threshold voltage. In Fig. 5, different sampling points are shown for five threshold levels and three sampling locations (C = 3). The sampling point (p1~p5) is adjusted by the programmable threshold voltage (Th = 0~4) and the dynamic sampling clock-edge (s = 0~2) due to the synchronized fractional sampling. Note that the location of the sampling clock-edge is periodic with C (i.e., 1->0->2->1->0->2->…).

If the sample point is above the high level of the input signal (p1) or below the low level of the input signal (p2), the output logic of the clocked-comparator is always zero (p1) or one (p2). However, if the sample point is within the high and the low voltage level (p3, p4, and p5), the output logic is not deterministic. The outcomes of the logic depend on the statistics of the bit pattern. In this paper, we assume the input signal is a PRBS whose logic transition is balanced. This means that the number of the four possible logic-transitions (one-to-one, one-to-zero, zero-to-zero, zero-to-one) is equally distributed in a long observation. With this assumption, the distribution of logic one and zero at p3 is expected to be 1:1. It is because the sample point (p3) is below the two logic-transitions (one-to-one and one-to-zero) and above the others (zero-to-zero and zero-to-one). Likewise, the logic distribution at p4 and p5 is expected to be 3:1 and 1:3, respectively. Therefore, the shape of the eye can be distinguished by the logic distribution.

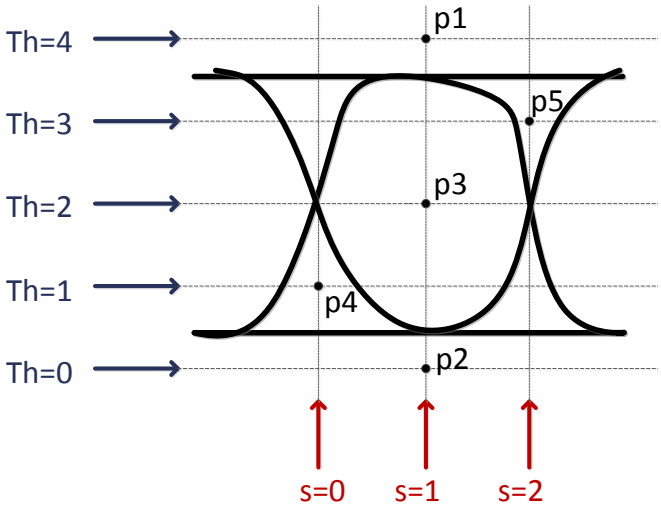


Fig. 5. Different sampling points in eye diagram by adjustable threshold level and synchronized fractional subsampling.

C. FPGA Logic

The monobit eye-reconstruction algorithm is implemented in FPGA logic. The block diagram of the FPGA logic is shown in Fig. 6.

The current sampling location is tracked and stored by updating a sequence every sampling clock (Discrete-time sequence generator). As described in the previous section, the time-location of the sampling clock-edge forms a periodic sequence depending on the frequency relationship parameterized by coprime C and D. In order to accumulate a logic distribution at a point, the corresponding threshold is fixed until a desired amount of the logics at the point is gathered. For example, to obtain the logic distribution at point p3 with 10 logic-samples, the threshold is fixed at level 2 for 30 cycles ($3 \cdot 10$). The parameter C is multiplied due to the periodicity of the sampling location (C-Counter). After the desired number of the samples are collected, the threshold is programmed to the next level (Vth generator). The logic distribution at each evaluated point is stored in the memory (Eye reconstruction unit).

The accuracy of the eye-reconstruction depends on 1) the time-resolution (C), 2) the number of threshold level (NTh), and 3) the number of logic-samples (L) for each sampling point. If the entire eye reconstruction is required, the total amount of memory will be $C \cdot NTh \cdot \lceil \log_2 L \rceil$ bits. Therefore, there is a tradeoff between the accuracy and the amount of resource.

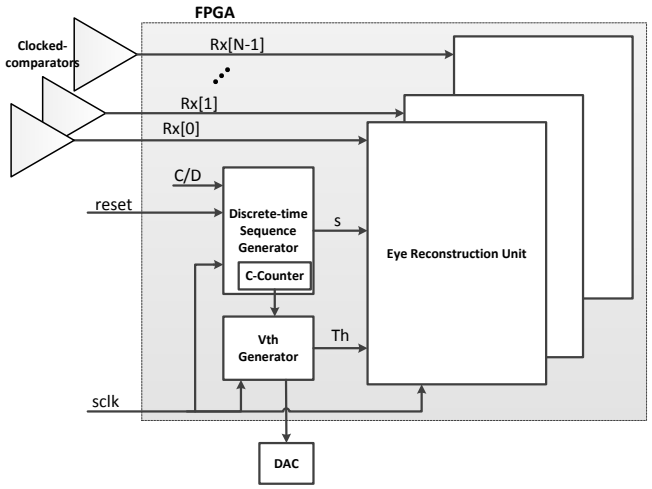


Fig. 6. Block diagram of FPGA logic.

V. Hardware Experiment

The FPGA generates 3.2Gbps NRZ PRBS test signal (length of sequence = $2^7 - 1$) and receives the output logic from the clocked-comparator. The sampling clock for the clocked comparator and the FPGA logic is chosen to have $C = 313$sampling time-location over the bit period ($1/f_b$) of the PRBS. We also choose $D = 3200 * 10$ for the subsampling factor, and the resulting sampling frequency would be $\frac{C}{D} \cdot f_b = \frac{313}{3200 \cdot 10} \cdot 3.2GHz = 31.3MHz$. In this setup, sub-picosecond resolution (0.9984ps) can be achieved.

In Fig. 7, the reconstructed eye-diagrams are compared with the input PRBS captured by an Agilent 81600D sampling oscilloscope. The reconstructed eye-diagrams are obtained by $NTh = 121$ threshold level with 0.6mV step and $L = 128$ number of logic-samples per a sample point. The FPGA stores the reconstructed eye-diagram in 313-by-121 array. To visualize the resulting logic distribution, the array is color-mapped. The driver is programmed with three different pre-emphasis. Fig. 7(a) compares the input signal without pre-emphasis and the corresponding reconstruction. Fig. 7(b) shows the input signal with 15% pre-emphasis magnitude and 100ps pre-emphasis duration and the corresponding result. Fig. 7(c) shows the input signal with 25% pre-emphasis magnitude and 200ps pre-emphasis duration and the corresponding result. The shapes of the reconstructed eye-diagram correspond well to the corresponding input waveform. For example, the pre/post transition overshoot and undershoot in the input waveform of Fig. 7(a) is presented in the corresponding reconstructed eye-diagram. Similarly, the input signal in Fig 7(c) is over pre-emphasized and its signal shape is tracked in the reconstruction. In this experiment, we can find the optimal pre-emphasis (Fig. 7(b)) by the reconstructed eye-diagram.

In Fig. 8, the typical rise and fall times and peak-to-peak jitter of the input signal are shown with the edge-highlighted reconstructed eye-diagram of Fig. 7(b). With a proper voltage swing and DC-offset at 3.2Gbps throughput, rise and fall times are typically about 45ps (20%~80%) and peak-to-peak jitter is about 30ps including 6σ random jitter. As shown in Fig. 8, the reconstructed eye-diagram is able to represent the timing-characteristics of the input signal.

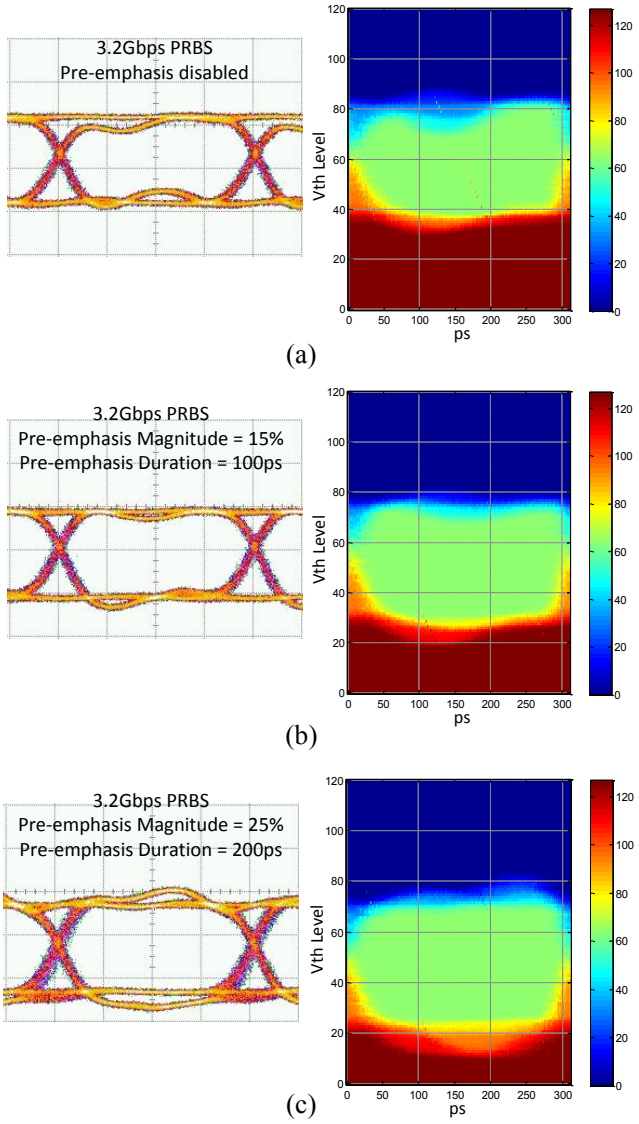


Fig. 7. 3.2Gbps PRBS input waveforms and reconstructed eye-diagrams for three different pre-emphasis settings of the driver.

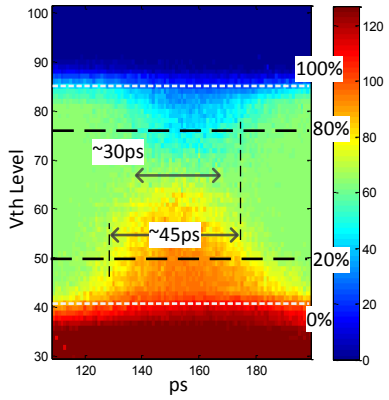


Fig. 8. Typical rise and fall times and peak-to-peak jitter of the input signal and reconstructed eye-diagram.

VI. Conclusion and Future Work

In this paper, we present a new multi-channel testing architecture for high-speed eye-diagram. The combined use of pin electronics and FPGA implementable reconstruction algorithm achieves sub-picosecond resolution for multi-Gbps eye-reconstruction with subsampling clock as well as high scalability of test system. The hardware measurement result verifies the reconstructed eye-diagram is well matched with the input waveform.

In our future work, a robust method to quantify the characteristics of reconstructed eye-diagram will be presented.

Acknowledgment

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