Low-Cost Multi-Channel Testing of Periodic Signals Using Monobit Receivers and Incoherent Subsampling

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Abstract— **This paper proposes a new method to reconstruct signal by a monobit receiver based on incoherent subsampling. The proposed method uses a time-variant threshold voltage for the monobit receiver to increase its amplitude resolution. By our methodology, the threshold voltage does not have to be synchronized with the input signal nor the sampling clock of the system. Hardware measurement with FPGA and high-bandwidth clocked-comparators shows that a low-cost multi-channel test is achievable by our method. The hardware measurement results show a square waveform and a sin wave waveform reconstruction.**

Index Terms— **Monobit receiver, analog-to-digital conversion, incoherent subsampling, frequency estimation.**

I. INTRODUCTION

MULTI channel RF test system has received attention, as it is expected to lead a significant increase in testing time and throughput. One of application of the multi-channel RF test system is testing multiple-input multiple-output (MIMO) systems. However, achieving accurate testing with high-resolution ADCs introduces high-cost in the multi-channel test system.

The effort on reducing the cost of ADCs motivates the development of single-bit or monobit receivers. The design and performance of monobit receivers for ultra-wideband communications are discussed in [1], [2]. The works, however, are restricted to over-sampling condition and symbol estimation for communication purpose.

In [3] and [4], high-precision eye-opening monitor (EOM) circuit and adaptive control scheme are developed. The combination of high-precision EOM and adaptive decision-point control scheme improves bit-error-rate (BER) [3]. In [4], a 10-Bs/s adaptive look-ahead decision feedback equalizer (LADFE) is used to measure eye-diagram and fabricated in 90-nm CMOS technology.

Successive-approximation register (SAR) ADC is an attractive design for low-cost and low-power ADC. The SAR ADC determines the level of input signal through a binary search algorithm. However, SAR ADC with high-resolution need a large capacitor array which limits the ADC dynamic performance.

In this paper, we consider a monobit receiver using clocked-comparator whose threshold voltage is time-variant to increase the resolution of the ADC. By comparing the time-variant threshold voltage, the level of input signal is estimated. With a carefully chosen combination of sampling frequency and threshold frequency, the input signal is reconstructed with high-resolution. In [5], a similar idea which exploits a periodic threshold voltage (ramp signal) to compare with the input signal has been proposed. This work, however, requires the threshold signal and the input signal to be synchronized. In other words, the phase relationship of the two signals is known during the measurement.

The main contribution of this paper is in proposing a low-cost hardware scheme of monobit receivers to reconstruct a high-speed RF signal using intelligent incoherent undersampling and signal reconstruction algorithms. Since the algorithm is based on incoherent sampling technique, the phase of the input signal, the sampling clock signal and the threshold signal do not have to be synchronized. This property simplifies the hardware setup for the signal testing. In addition, the application of our algorithm is not constrained to digital bit sequences. It can also reconstruct any arbitrary periodic signal. Thus, the algorithm extends to testing RF harmonic signals.

The overall architecture of the proposed method is presented in Section II. The detailed signal reconstruction algorithm is described in Section III. The optimal choice of the sampling frequency and the frequency of threshold signal is studied in Section IV. In Section V, hardware measurements with a FPGA board and a clocked-comparator show the results of the reconstruction.

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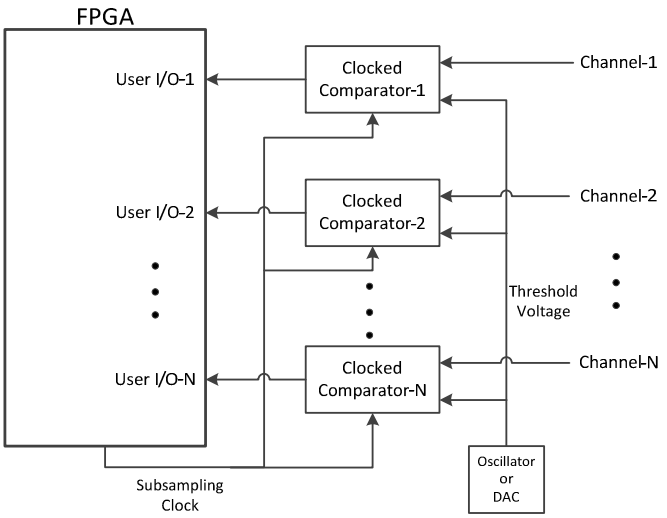

Fig. 1. Block diagram of the proposed multi-channel monobit receiver test system.

II. Multi-channel Monobit Receiver Architecture

Fig. 1 shows the proposed multi-channel monobit receiver architecture. In each channel, a single clocked-comparator converts the input test signal into two logic-levels ('High' or 'Low') for an FPGA. A time-variant threshold signal is applied to the clock-comparator and compared with the input test signal. When the amplitude of the input test signal is greater than that of the threshold signal, the output of the clock-comparator is 'High'. In the opposite case, the output is 'Low'. The threshold signal can be generated from an oscillator which produces a sin wave or from a DAC which can produce any arbitrary waveform. The constraint for the threshold signal is, however, that it should be periodic and its fundamental frequency should be carefully chosen for the signal reconstruction. In addition, the peak-to-peak of the threshold signal embraces that of the input signal. This condition guarantees that the input test signal is fully covered by the threshold signal.

The FPGA samples the bit stream with a subsampling clock which is also shared with the clock-comparator. A time-delay between the sampling clock of FPGA and the sampling clock of the clocked-comparator is adjusted to compensate the propagation delay of the clocked-comparator.

The key merit of our reconstruction algorithm is that the threshold signal is not necessarily to be synchronized with the input test signal nor the sampling clock. The phase of the threshold signal is compensated in the back-end digital process. Hardware measurements in Section V validate the performance of the algorithm.

In this paper, we focus on the signal reconstruction and its performance on a single channel. We assume the input test signal is AC-coupled, therefore, it is reasonable for the threshold signal to be also AC-coupled. The threshold signal is assumed to be an ultra-clean sinusoidal wave whose exact amplitude and frequency is known. The phase of the threshold signal is, however, unknown. The amplitude of the threshold is assumed to be large enough to cover the peak-to-peak of the input test signal. In addition, the input test signal is wide-sense stationary (WSS) which guarantees the spectrum of the input test signal does not vary with respect to time.

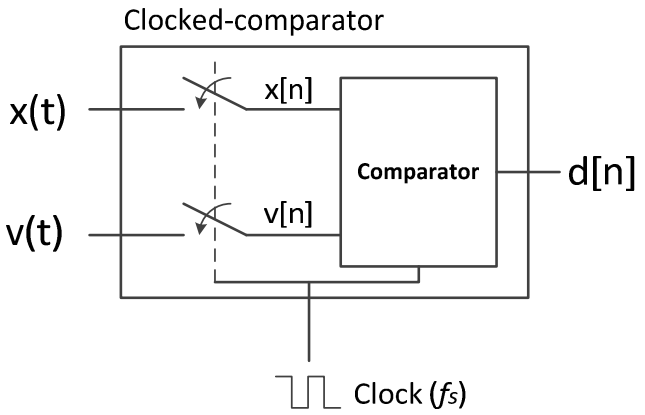

Fig. 2. Conceptual diagram of a clocked-comparator.

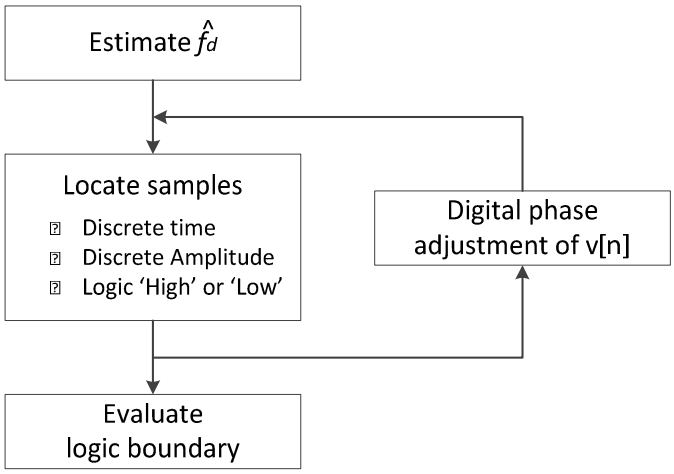

Fig. 3. Flow of the proposed signal reconstruction algorithm.

III. Detailed Signal Reconstruction

Before illustrating the proposed algorithm, the notation of this paper is denoted as followings:

$f_s = \frac{1}{T_s}$: sampling clock frequency(Hz)
f_{th}: threshold signal frequency(Hz)
x(t): input test signal
$x[n] = x(nT_s)$: n-th sample of input test signal
v(t): threshold signal
$v[n] = v(nT_s)$: n-th sample of threshold signal
d[n]: n-th sample of clocked comparator output
$\hat{f}_d$: discrete fundamental frequency of input test signal

The conceptual diagram of a clocked-comparator is shown in Fig. 2. The input test signal (x(t)) and the threshold signal (v(t)) are sampled at the rising edge of the sampling clock with the

frequency *fs*. The two sampled points are compared and the output logic level is determined as following:

$$d[n] = \begin{cases} 1, & \text{if } x[n] \geq v[n] \\ 0, & \text{if } x[n] < v[n] \end{cases} \quad (1)$$

Note that '1' and '0' represent a voltage level, not the actual voltage value.

The signal reconstruction by the proposed algorithm involves several steps as shown in Fig. 3. The brief overview of the algorithm is as follows: 1) estimate the discrete fundamental frequency of the test input signal, 2) locate the samples over the discrete fundamental period with its discrete time, amplitude and logic level, and run iteratively while the digital phase of the threshold signal, v[n], is adjusted with a cost function. 3) interpolate the boundary points of logic '1' and '0'.

A. Step1: Estimate $\widehat{f_d}$

In [6], accurate discrete frequency estimation using the frequency shifting technique is presented. We use the frequency shifting technique to improve the resolution of the discrete fundamental frequency of the input test signal. The idea of the frequency shifting method is to shift (or modulate) the discrete spectrum of incoherent sampling to fit into the DFT frequency bins. When the discrete frequency of the fundamental tone is not exactly on a DFT bin, a spectral leakage happens into the neighbor bins. By shifting the fundamental tone close to the DFT bin, the magnitude of the corresponding DFT bin would increase.

To compute the fundamental discrete frequency ($\widehat{f_d}$) of the input signal, the ground reference is applied to obtain a two-bit resolution samples of the AC-coupled input test signal.

B. Step2: Locate samples

In this step, the amplitude-resolution of the input test signal is improved by comparing with the sinusoidal threshold signal. Since the amplitude and the frequency of the threshold signal are given, we can draw a virtual threshold signal without its exact phase.

While the phase of the threshold signal is adjusted in the next process, we assume the phase is known for the following example. Fig. 4(a) shows an example of a square wave input test signal and a sinusoidal threshold signal. When the input test signal is greater than the threshold signal, the clocked-comparator generates the samples of logic '1'. The grey downward-pointing triangles represent the samples of logic '1'. Similarly, the black upward-pointing triangles represent the samples of logic '0'. Note that the logic of the samples is flipped when the threshold signal crosses over the input test signal. The dotted-circles emphasize the boundary points of the flipping logic. The frequency of the threshold signal is carefully chosen to have a long common period with the input test signal. Otherwise the threshold signal travels only a few paths over the test signal, which reduces the resolution of the reconstruction.

Once the $\widehat{f_d}$ is estimated in the previous step, the discrete time of v[n] is determined over the fundamental period as shown in Fig. 4(b). The time location of the k-th sample is remapped within the fundamental period as

$$t_d[k] = mod\left(k, N/\widehat{f_d}\right) \quad (2)$$

where *N* is the total number of samples.

The discrete amplitude of x[n] is evaluated by the boundary points of logic '1' and '0'. In the example, the nine dotted-circles which indicate the boundary points imply the shape of the input test signal. As the number of samples increases the time and amplitude resolution of the boundary points increases as shown in Fig. 4(c).

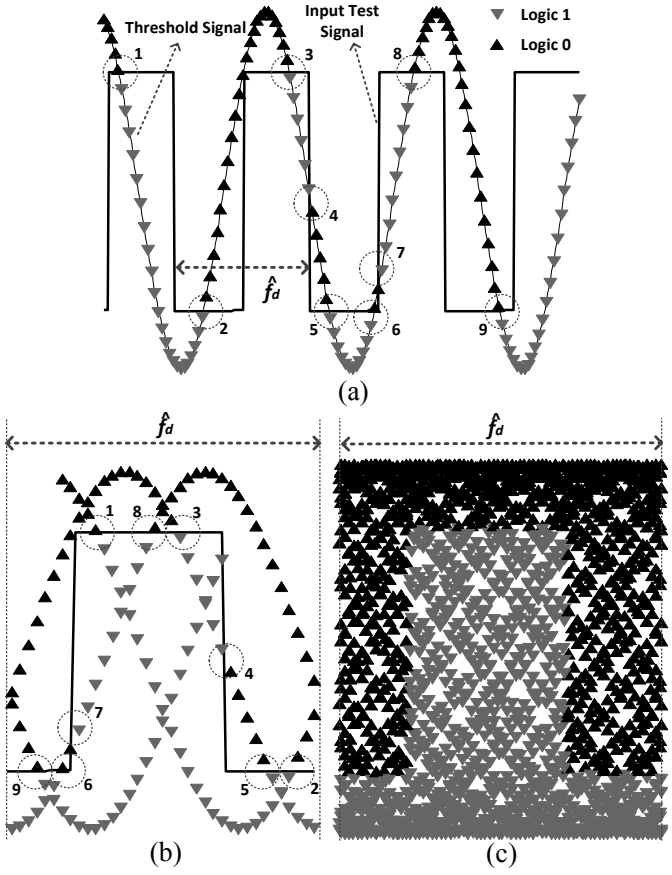

Fig. 4. (a) A square wave and a sinusoidal threshold signal are plotted with the output logic of the clocked-comparator over the time axis. (b) The samples are remapped over the estimated $\widehat{f_d}$. The circles indicate the flipping points. (c) More samples are plotted.

C. Step3: Digital phase adjustment

The digital phase adjustment is achieved by iteratively changing the phase of the virtual threshold signal. Note that the phase of the true threshold signal is unknown. If the phase of the virtual threshold signal does not match the phase of the true threshold signal, the mismatch error occurs at the boundary points. Fig. 5 shows the previous example with an incorrect digital phase offset. Comparing with Fig. 4(b), the incorrect digital phase of the virtual threshold signal introduces the error

from the boundary points to the input test signal as shown in Fig. 5(a). As a result, the boundary points do not accurately cover the input test signal in Fig. 5(b). Note that the envelopes of logic '1' and logic '0' exactly meet at the input test signal in Fig. 4(c), while they cross over each other in Fig. 5(b).

The best phase of the virtual threshold signal is selected when the following cost function is minimized.

$$cost(\phi) = \int_0^{\widehat{f_d}} env_0(u,\phi) - env_1(u,\phi)du \qquad (3)$$

where ϕ is the digital phase of the virtual threshold signal and u is a dummy variable in $[0, \widehat{f_d}]$. The function $env_0(u,\phi)$ is the envelope of the logic '0' samples and $env_1(u,\phi)$ is the envelope of the logic '1' samples. The shape of the function $env_0(u,\phi)$ and $env_1(u,\phi)$ depends on ϕ.

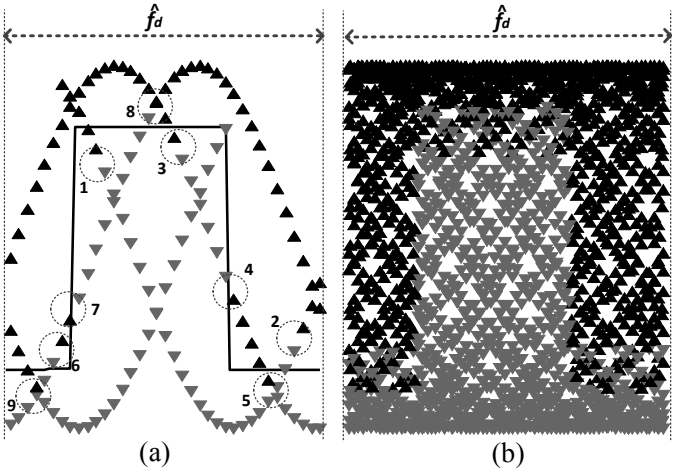

Fig. 5. Incorrect digital phase of the threshold signal produces errors.

D. *Step3: Evaluate logic boundary*

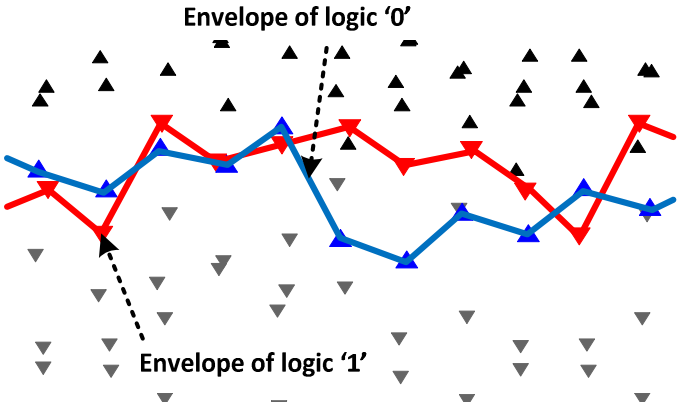

Fig. 6. The logic boundary is evaluated by enveloping.

The final step of the algorithm is to evaluate the logic boundary. The logic boundary roughly indicates the input test signal. The envelope of the logic '0' (logic '1') samples is obtained by choosing the minimum (maximum) value in a given time window. Fig. 6 shows an example to evaluate the logic boundary. Evaluating the logic boundary with a short time window can improve the resolution over the time. However, the logic boundary can be over-evaluated with a too short time window. Thus, the size of time window should be carefully chosen based on the number samples.

IV. Frequency Selection

Given the input test signal, the frequencies of the sampling clock and the threshold signal determine the resolution of the reconstruction. As discussed in the previous section, the frequency relationship between the input test signal and the threshold signal decides the number of the distinct paths that the threshold travels over $\widehat{f_d}$. As the number of the distinct paths increases, more number of amplitudes of the threshold signal is compared with the input test signal. Furthermore, the frequency relationship between the sampling clock and the input test signal impacts on the time resolution of the reconstruction.

All the relationship of the three frequencies (clock, input, and threshold) is desired to have a long common period. If they have a short common period, it takes a short time (or few samples) to sample the same point of the input test signal with the same point of the threshold signal. It means that the redundant information is obtained in a few samples. To avoid a short common period, we choose the frequencies of the sampling clock and the threshold signal with the fundamental frequency of the input test signal as following:

$$f_s = \frac{\prod_{i=1}^{P_1} \alpha_i}{\prod_{i=1}^{S_1} \beta_i} f_d \qquad (4)$$

$$f_{th} = \frac{\prod_{i=S_1+1}^{S} \beta_i}{\prod_{i=P_1+1}^{P} \alpha_i} f_d \qquad (5)$$

where f_s and f_{th} are the frequencies of the sampling clock and the threshold signal, respectively. The fundamental frequency of the input test signal is denoted by f_d. Note that f_d is the continuous frequency whereas $\widehat{f_d}$ is the discrete frequency related to the total number of samples *N*. The integers $\alpha_1, \dots, \alpha_P$ and $\beta_1, \dots, \beta_S$ represent the prime numbers. The set $A = \{\alpha_1, \dots, \alpha_P\}$ and $B = \{\beta_1, \dots, \beta_S\}$ are chosen to be disjoint, $A \cap B = \emptyset$, which leads

$$f_s = \frac{\prod_{i=1}^{P} \alpha_i}{\prod_{i=1}^{S} \beta_i} f_{th} \qquad (6)$$

without any cancelations.

The time-resolution of the reconstruction is determined by $\prod_{i=1}^{P_1} \alpha_i$ and f_d. This is because the number of the time-stamps of the sample points in the fundamental period is $\prod_{i=1}^{P_1} \alpha_i$. Thus, the time-resolution is

$$res_t = \frac{1}{f_d \cdot c} \qquad (7)$$

V. Hardware Experiment

The measurement setup is shown in Fig7. HMC874LC3C from Hittite is a clocked-comparator supporting 20Gbps clock operation and 10GHz input bandwidth. The output waveform

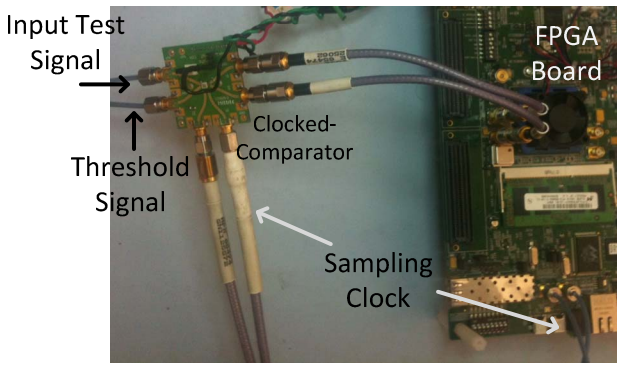

Fig. 7. Hardware measurement setup.

of the clocked-comparator is captured by an FPGA board. We use a Virtex6 evaluation board.

Two types of input test signals are measured: a digital square wave and a sin wave. The high-speed digital square wave of 1.6GHz frequency is generated. For the sampling clock,

$$f_s = \frac{163 \cdot 223}{977 \cdot 983} 1.6\text{GHz} \approx 60.557\text{MHz}$$

is chosen as the sampling frequency. The frequency of the sinusoidal threshold signal is chosen as

$$f_{th} = \frac{163 \cdot 223 \cdot 991^2}{977 \cdot 983 \cdot 997^2} 1.6\text{GHz} \approx 59.8303\text{MHz}$$

Similarly, the frequencies of the sampling clock and the threshold signal are chosen for the 1GHz sin wave with different prime numbers as followings:

$$f_s = \frac{211 \cdot 223}{977 \cdot 983} 1\text{GHz} \approx 48.9937\text{MHz}$$
$$f_{th} = \frac{211 \cdot 223 \cdot 991^2}{977 \cdot 983 \cdot 997^2} 1\text{GHz} \approx 48.4057\text{MHz}$$

To cover the input test signal, the peak-to-peak of the threshold signal is set to 600mV. The threshold signal is applied externally without synchronization.

Fig. 8 shows the cost function over the adjusted digital phase in the case of the square wave. While the phase is swept over the range [-180, 180] degree, the cost function is computed. The cost function has the minimum value at the phase of -124.4 degree. The threshold signal of phase -124.4 degree produces least mismatches on the logic boundary.

Fig. 9 and Fig. 10 compare the input test signal and the reconstructed signal. The envelopes of the logic '1' and logic '0' are plotted together. The result of the square wave input test signal shows the reconstructed signal has a minor distortion on the waveform. However, the reconstruction accurately captures the edge of the square wave and the amount of jitter is very close to the signal measured by the high-speed oscilloscope. In sin wave measurement, the proposed algorithm reconstructs the waveform with better accuracy.

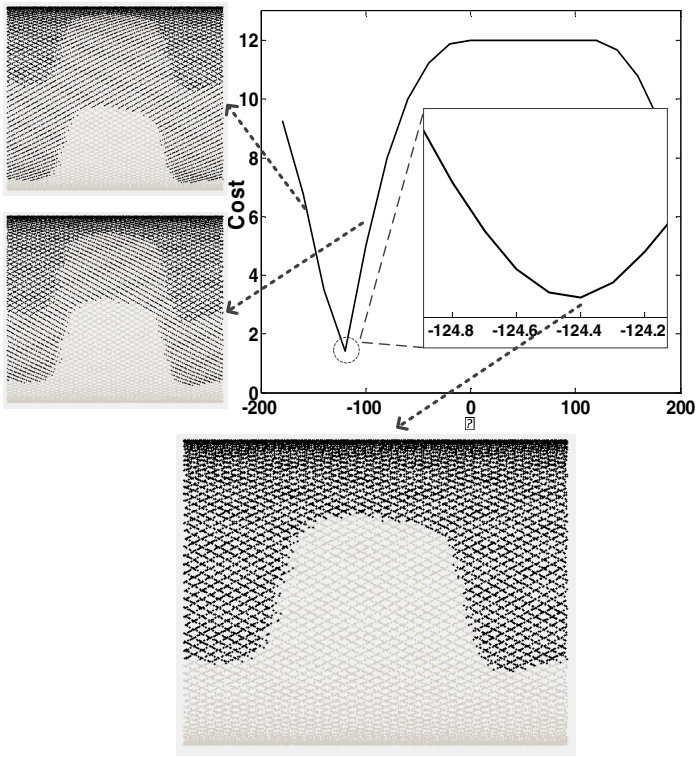

Fig. 8. Cost function and remapped samples.

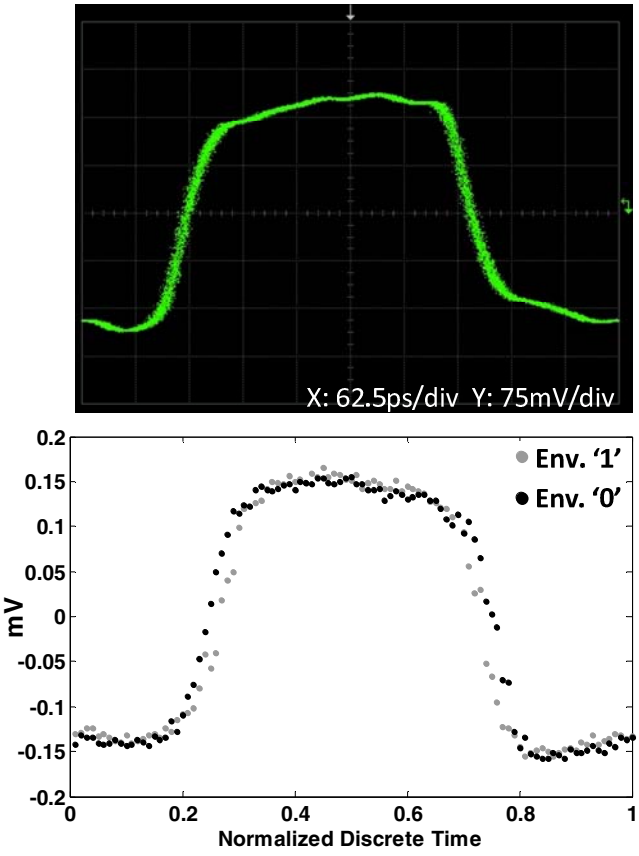

Fig. 9. Square wave input test signal and reconstruction.

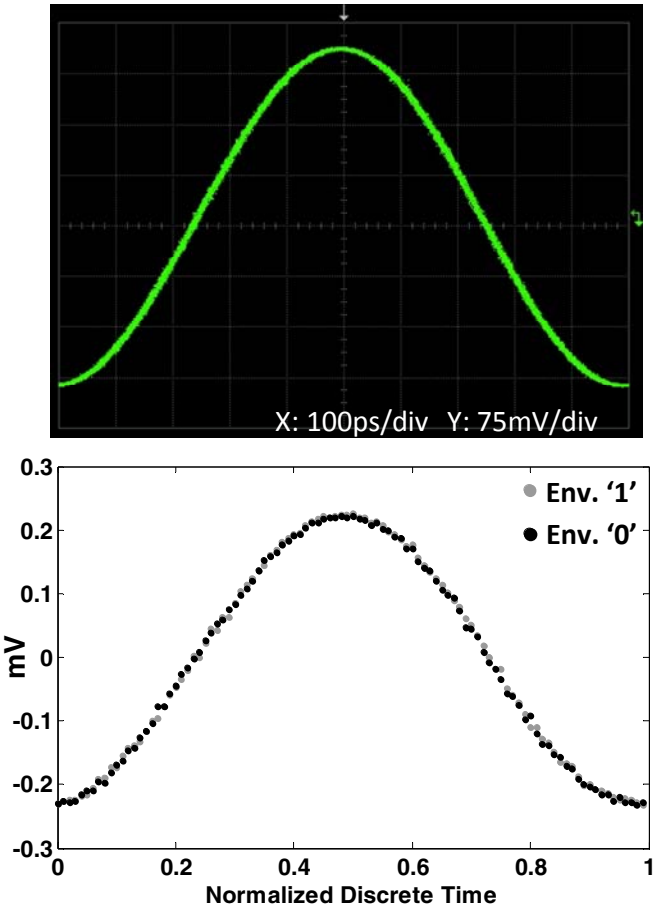

Fig. 10. Sin wave input test signal and reconstruction.

The results show the frequency of the sampling clock and the threshold signal does not require fast to reconstruct a high-speed input test signal. The input test signals measured in this paper are around 20 times faster than the sampling clock.

The following table summarizes the time-resolution (TR), the test-time (TT) and the number of samples (NS) for the hardware measurements.

TABLE I
TIME PARAMETER FOR HARDWARE MEASUREMENT

	TR (ps)	TT (μs)	NS
Square wave	0.0172	338	20·1024
Sin wave	0.0213	418	20·1024

VI. CONCLUSION AND FUTURE WORK

In this paper, a new signal reconstruction architecture and algorithm is introduced. The hardware architecture with monobit receivers based on incoherent subsampling is expected to reduce the cost of multi-channel testing. The use of a time-variant threshold signal increases the resolution of the signal reconstruction. The hardware measurement shows the input signal is reconstructed in high-resolution and high-accuracy without a synchronized threshold signal, which reduces the hardware complexity. In addition, the results show the reconstruction is achievable with low-speed sampling clock and threshold signal.

In our future work, more robust method to reconstruct the input signal from the logic boundaries will be studied. The research to reduce the test-time will also be done. In addition, more algorithms for eye-diagram extraction will be included. Multi-channel testing system will be implemented in hardware with the proposed algorithm.

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