High Average-Efficiency Power Amplifier Techniques

Jason Stauth, U.C. Berkeley Power Electronics Group
Overview

- Application Space: Efficient RF Power Amplifiers
- PA Fundamentals, Polar/ET Architectures
- Challenges with Polar/ET
- Research Directions
- Direct Digital Modulation
- Pulse-Density Modulation
Power Amplifier Fundamentals

Edge Constellation: 3π/8, rotated 8-PSK
Linear Power Amplifier (PA)

- Active transconductance device
- Input matched to previous stage
- Output (antenna) impedance transformed to increase power gain
- Small-signal model close to common source amplifier
Nonlinear PA

- Active device operates as a switch
- Approx LTV System
- Voltage waveform constrained (also consider current waveform)

- Class-F
  — Frequency Domain
  — Impedance Design

- Class-E
  — Time domain
  — Impulse Response design

- Class E/F ZVS Amplifiers, Kee et al., MTT '03
The Point…

- Nonlinear PAs can’t do amplitude modulation
- Linear PAs can do amplitude modulation, but are inefficient

\[ \eta_A \approx \frac{1}{2} \frac{V_a^2}{V_{dd}^2} \quad \eta_B \approx \frac{\pi}{4} \frac{V_a}{V_{dd}} \quad \eta_S \approx \frac{V_a}{V_{dd}} \]
Average Efficiency

\[ \eta_{avg} = \frac{E_{load}}{E_{supply}} = \frac{\int_{-\infty}^{\infty} g(P_L) \cdot P_L dP_L}{\int_{-\infty}^{\infty} g(P_L) \cdot P_{supply}(P_L) dP_L} \]

\[ = \frac{\int_{-\infty}^{\infty} g(P_L) \cdot P_L dP_L}{\int_{-\infty}^{\infty} g(P_L) \cdot \frac{P_L}{\eta(P_L)} dP_L} \]

<table>
<thead>
<tr>
<th>PA Class:</th>
<th>Class A</th>
<th>Class B</th>
<th>Nonlinear PA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Efficiency:</td>
<td>0.78%* / 9.2%**</td>
<td>14.46%</td>
<td>18.21%</td>
</tr>
</tbody>
</table>

*constant bias current  
**variable bias current
Polar and Envelope Tracking Transmitters

- Supply regulation synchronous with RF Envelope

\[ \eta_{avg} = 62.5\% \]


V = F(I, Q) = I \cdot \cos(\omega t) + Q \cdot \sin(\omega t)

V = F(\rho, \phi) = \rho \cdot e^{j(\omega t + \phi)}

- Many (most?) implementations don’t use an efficient supply modulator →
- efficiency gains from using nonlinear PA
Envelope Tracking

- Linear (class-AB) PA
- Efficient supply modulator (linear reg doesn’t make sense)

Operate at max PAE point
Challenges

- Bandwidth
- Peak-average power ratio
- Time alignment
- Distortion (AM-AM, AM-PM)
- PSRR

<table>
<thead>
<tr>
<th>System</th>
<th>Bandwidth (MHz)</th>
<th>Peak-Average Power Ratio (dB)</th>
<th>Power Control Range (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSM</td>
<td>0.20</td>
<td>0</td>
<td>30</td>
</tr>
<tr>
<td>EDGE</td>
<td>0.20</td>
<td>3.2</td>
<td>30</td>
</tr>
<tr>
<td>WCDMA</td>
<td>3.84</td>
<td>3.5–7</td>
<td>80</td>
</tr>
<tr>
<td>cdma2000</td>
<td>1.23</td>
<td>4–9</td>
<td>80</td>
</tr>
<tr>
<td>802.11a/g</td>
<td>18.0</td>
<td>6–17</td>
<td>—</td>
</tr>
</tbody>
</table>
Project Directions

Wideband Switching Regulators

Hybrid Linear-Switching Regulators

Direct Nonlinear Modulation Transmitters
Wideband Switching Regulators

- Envelope Tracking Architecture
- Wideband: 20MHz Envelope bandwidth
- High switching frequency
- High PSRR PA

![Diagram of Wideband Switching Regulators]

- Control & PWM Switching Regulator
- Probability density function
- PA Efficiency with dynamic supply
- Probability
- Efficiency

- Baseband
- IF upconversion
- LO
- RF
- Vdd
- Envelope Detect
- RF-Out
Challenge: Power Supply Rejection

- Supply noise can mix into the RF spectrum, degrading SNR, violating spectral masks (ACPR)

- New Concept: design for high PSRR

-Stauth, Sanders, "Power supply rejection for RF amplifiers," (RFIC) Symposium, June 2006
Results: MTT Oct ‘07

- Supply-Signal mixing term:

\[ A_{11}(jw_a, jw_b) = y_S \cdot \frac{gmo_{11}K_1 + 2y_2K_2 + 2gm_2K_3 - 2gmb_2K_4}{K_0} \]

\[ PSRR = dB \left| \frac{gm_1}{gmo_{11}K_1 + 2y_2K_2 + 2gm_2K_3 - 2gmb_2K_4} \right| \]

PSRR = sideband in dBc for 1V (0dBv) supply noise tone

![Graph showing PSRR values for different configurations: gmo11, gmo11+go2, gmo11+go2+C2.](image1)

![Graph showing the power spectral density with calculated and measured data, highlighting the supply ripple sidelobes.](image2)
Hybrid Linear-Switching Regulators
Hybrid Regulator Paradigm

Series Hybrid

- Decouple bandwidth-efficiency (audio, AVS digital, PA supply)
- Fast linear block: *(supply dynamic output voltage, attenuate switching regulator harmonics)*
- Slow switching block: *(efficient, low cost)*
- Series hybrid drawbacks: low Vdd efficiency, headroom issues

Parallel (shunt) Hybrid
Parallel Hybrid Operation

- Linear Stage: Voltage Follower (Class AB LDO)
- Switching Stage: Current source
- Traditional: $\langle i_{SR} \rangle = \langle i_{LOAD} \rangle$
- Previous work: Optimize in the frequency domain

- Yousefzadeh, et al. ISCAS ‘05, PESC 06.
- P. Midya et al. PESC, ‘00.
This Work: Optimize in the Time Domain

- Fundamental: many signals may share same power spectrum
- Phase of signals not represented \(\rightarrow\) can be critical for max efficiency in the time domain
- Consider strong nonlinearities in conversion from Cartesian to polar representation
Interesting Conclusions

• Traditional method with $\langle \! \langle i_{SR} \rangle \! \rangle = \langle \! \langle i_{LOAD} \rangle \! \rangle$ is suboptimal

• Optimum $isr$ is a function of $Vdd$, and dynamics of the modulation signal

• Power savings potentially very large for high PAPR signals, high $Vdd$
Future Work

- Adaptive optimization
- Performance tuning
Digital Pulse-Density Modulation
This work:
1-Bit Linear Transmitter

- PA at ‘max power’ or ‘off’
- Inherent linearity
- Improved efficiency in power backoff…
Pulse Density Modulation Process

- AM process $\rightarrow$ Extra harmonics
- Tradeoff between oversampling ratio & Q
  - Out of band spectrum
  - Efficiency
- Noise shaping: digital $\Sigma\Delta$
- Conclusions
  - No major efficiency advantage with $Q<\sim 5-10$
  - Linearity may be the compelling factor
  - (almost) pure digital implementation!
  - Need to run PDM process *as fast as possible*

![Diagram showing power spectrum, filter profile, and carrier with DSB harmonics.](Image)
PDM Process

- Sigma-delta
  \[ v(t) \xrightarrow{\Sigma} z^1 \xrightarrow{\Sigma} \text{quantizer} \xrightarrow{\text{PDM}} y(t) \]

- Error feedback
  \[ v(t) \xrightarrow{\Sigma} \text{quantizer} \xrightarrow{G(\alpha)-1} \xrightarrow{\Sigma} y(t) \]

Spectrum:
- bandpass in nature
- Amplitude modulation
- Noise Shaping
PDM Process

- Modulate at fraction of carrier frequency
  → out of band harmonics
PDM Process

- Modulate at fraction of carrier frequency
  → out of band harmonics
PDM Process

- Modulate at fraction of carrier frequency
  → out of band harmonics
Class-D PA

- Conventional timing, control
- Series-Resonant Filter $\rightarrow$ block out of band harmonics
- High impedance out of band $\rightarrow$ reduce power drawn from supply for ‘wasted’ energy
Architecture

- Cartesian Representation
  - Noise-Shaped PDM amplitude modulation
  - Independent I-Q processing/upconversion
  - Class-D PA
  - Series resonant bandpass filter/transformer

This work
Behavioral Verification

- Ideal Components, PDM process
- Passive network Q~30
- Vdd=1.0V (assume 90nm CMOS)
Ideal $\rightarrow$ no losses in switches, passives
Carrier Fundamental Linearity

Simulation, expt show good linearity vs pulse density
IM3 comparable to good linear PA (range of -20dBc to -40dBc)
Predistortion likely to improve linearity further

Output Voltage Amplitude vs Code

\[
y = 7.27E-04x^3 - 1.37E-02x^2 + 3.61E-01x
\]
Class D PA, 90nm CMOS, Spectre Sim, Q~15 in passives
2-tone test
Conclusions

Efficiency stays high in power backoff

Future analysis: comparison of series resonant to parallel resonant output filters for class-D PAs

High linearity, compelling argument for this architecture
Implementation

Two chips: Modulator and Class D PA

90nm CMOS, 1.0V voltage, wirebond chip-on-board
Multiple stages: RF PDM and Baseband sigma-delta
Tradeoff oversampling for power consumption
Still have 10-100x oversampling for most standards (edge, Bluetooth, WCDMA, 802.11x)
PDM Process

\[ G(z) = 1 - 2.5z^{-1} + 2.5z^{-2} - z^{-3} \]
Use 2.0V to drive for higher output power
Maximum Voxide=1.0V
No resonant switching: need accurate control of gate voltage
Recycle current used by high-side switches (excess goes to digital processing block)
Results

Program I/Q waveforms into FPGA
Downconvert/process signals with NI PXI box running labview

Results → show linear downconverted I/Q waveforms
Two-tone spectrum

0mV tones with 2MHz pacing at 1.95GHz carrier
0MHz of noise shaping is functional, noise peaks 50MHz from carrier at fs/2
LO leakage tuned with signal offset
802.11a, 64QAM OFDM Waveform

0mV tones with 2MHz pacing at 1.95GHz carrier
0MHz of noise shaping is functional, noise peaks 50MHz from carrier at fs/2
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WCDMA Spectrum
References


