Luis Francisco

Contact Information

Electrical and Computer Engineering Department
North Carolina State University
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Qualifications

Open to new challenges. Self-learner, capable of working independently and under pressure with minimum supervision. Reliable, highly organized and responsible.

Research Interests

Machine Learning for Electronic Design, Digital IC Design, and Architectures for ML.

Education

North Carolina State University, Raleigh, NC

Ph.D. in Electrical Engineering, Fall 2017-Current

- Advisors: Dr. Paul Franzon

University of Puerto Rico at Mayaguez, Mayaguez, PR

M.S. in Electrical Engineering, Fall 2012

- Topic: *Techniques for Spectral Discrimination of Noise Sources in Integrated MOSFETs*
- Advisor: Dr. Manuel Jiménez

Pontificia Universidad Católica Madre y Maestra, Santiago, Dominican Republic

B.S. in Electronic Engineering, 2007

Industry Experience

Machine Learning Technical Engineer Intern May 2019 - August 2019
Machine Learning for IC Physical Verification including short detection and computing resources management
Synopsys Inc, Raleigh NC

Machine Learning for DFM Technologies Intern May 2018 - August 2018
Apply Machine Learning to Design for Manufacturing problems including CMP and Lithograpy Hotspot Detection
GlobalFoundries, Santa Clara CA

Digital Design Engineer May 2016 to July 2017
Hardware design for Xilinx FPGA's and embedded Software design for Zynq SoC platform
Verluz LLC / Pacific Advance Technology, Mayaguez PR / Solvang CA

Embedded Software and Hardware Designer 2010-2012
Designer and developer of signal conditioning system, automation with Microcrontrollers and solar tracker algorithms and motor controls.
Freelancer for company in Atlanta, GA

Research Experience

Research Assistant August 2017 - current
NC State University - CAEML Group
Topic: *Explore the feasibility of applying machine learning to the DRC problem, ASIC backend flow and PPA modeling*
Supervisor: Dr. Paul Franzon

Research Assistant May 2016 to May 2017
Puerto Rico at Mayaguez, Mayaguez PR
Topic: *Algorithms for Computer Vision Using FPGAs*
Supervisor: Dr. Manuel Toledo

Research Associate Sept 2012 to January 2016
Research Program in Applied Electronics and Intelligent Systems
Pontificia Universidad Católica madre y Maestra, Santiago Dominican Republic
Major tasks: *Lead and collaborate in several projects in Power Electronics, Solar Energy and Remote Sensing. Supervise undergraduate research students.*

Research Assistant October 2009 to August 2012
University of Puerto Rico at Mayaguez and Texas Instruments, Mayaguez PR
Topic: *Noise Characterization and Automation Test for Integrated MOSFET's*
Supervisor: Dr. Manuel Jiménez

Selected School Projects

- **ASIC Design** of a two layers Convolutional Neural Network hardware. The design was implemented in Verilog RTL optimizing the delay area product.
- **ASIC Verification** of LC3 pipelined instruction set microprocessor. Including a layered SystemVerilog testbench, functional coverage analysis, assertions, and code coverage.
- **Computer Architecture:** Design and implement a simulator for a superscalar microprocessor. The simulator was written in C++ and included multiple floating point and integer execution units.
- **Physical Design** on an ARM Cortex-M0 SoC. The back-end was completed using Synopsys tools, and the design was optimized for delay area product. flow on an ARM CORTEX-M0 SoC.
- **FPGA hardware** accelerator to optimize real-time computer vision algorithms for object detection.

Relevant Skills

- **Computer Programming:** C, C++, Python, Keras API, TensorFlow Matlab, UNIX shell scripting, Assembly (x86, ARM, ASM for: MSP430, AVR, PIC and 8051 Microcontrollers) and Tcl Scripting.
- **CAD:** Vivado, Vivado HLS, Quartus, Cadence and Synopsys Tools.
- **HDL:** VHDL, Verilog and SystemVerilog.
- **OS**: Linux, Embedded Linux, Petalinux, OS X and MS Windows.

Publications

1. **L. Francisco**, R. Mao, U. Katakamsetty, P.Verma and R. Pack, "Multilayer CMP hotspot modeling through deep learning," 2019 SPIE Design-Process-Technology Co-optimization for Manufacturability XIII, San Jose, CA, 2019.
2. **L. Francisco** and M. Jiménez, "Parametric Model Calibration and Measurement Extraction for LFN Using Virtual Instrumentation," 2013 14th IEEE Latin American Test Workshop - LATW, Cordoba, 2013, pp. 1-6.
3. D. Soltero, **L. Francisco**, and E. Ortiz-Rivera, "Optimal Control for Buck Converter with PV module," in Center for Power Electronics Systems (CPES), 2010 Annual Conference, Blacksburg, VA, 2010.

Others Activities	• **Reviewer** for IEEE International Midwest Symposium on Circuit and Systems: IEEE MWSCAS 2017 Boston MA and IEEE MWSCAS 2018 Ontario Canada

Selected Awards and Honors	NC State University Provost's Doctoral Fellowship	NCSU, 2017
	Electronic Engineer - Cum Laude	PUCMM, 2003

References Excellent references available upon request