Hakki M. **Torun**

455 14th ST NW, Unit 545, Atlanta, GA, 30318, USA

(+1) 404-528-5943 | htorun3@gatech.edu | hakkimerttorun

Education

Georgia Institute of Technology — *Atlanta, GA, USA*
PhD Student, Electrical Engineering — *Aug. 2016 - PRESENT*

- Advisor: Madhavan Swaminathan
- Thesis: Bayesian Learning and Optimization for High-Performance Microelectronic Packaging

Georgia Institute of Technology — *Atlanta, GA, USA*
MSc, Electrical Engineering *(GPA: 3.81/4.00)* — *Aug. 2016 - May. 2019*

Bilkent University — *Ankara, Turkey*
BSc, Electrical and Electronics Engineering *(GPA: 3.80/4.00)* — *Sep. 2012 - Jun. 2016*

Research Experience

Intel Corporation — *Chandler, AZ, USA*
Analog Engineer Intern — *May 2019 - Aug. 2019*

- Developed a novel method to ensure broadband S-Parameters that are predicted through neural networks are causal and passive. The technique end-to-end trains the neural network to ensure convergence to a causal and passive parametric representation of S-Parameters that maximizes prediction accuracy.
- Worked on electromagnetic domain decomposition to decrease CPU time for 3D EM simulations of microelectronic packages.

IBM Corporation — *Austin, TX, USA*
Intern, Signal Integrity Analysis for High-Speed Server Busses — *May 2018 - Aug. 2018*

- Developed a novel machine learning algorithm, *Bayesian Active Learning using Dropout*, for fast & accurate uncertainty quantification of high-speed channel signaling to quantify effect of manufacturing tolerances. The developed method is used to ensure channel compliance at the worst case scenario, calculate expected eye diagram characteristics and generate sensitivity analysis.
- Modelled and analyzed motherboard pin area wiring structures using full-wave EM solvers.

Center for Advanced Electronics Through Machine Learning — *Atlanta, GA, USA*
Graduate Research Assistant (PI: Madhavan Swaminathan) — *Feb. 2017 - PRESENT*

- Research on developing domain-specific Bayesian learning based models and algorithms for data efficient statistical modelling, optimization, design space exploration and uncertainty quantification of electronic systems.
- Main focus is on learning the mapping between high-dimensional input and output parameters in the scarce data regime by developing novel methods based on active learning, Gaussian processes and convolutional neural networks.
- Application areas include signal/power integrity of high-speed parallel and SerDes channels at PCB, package and interposer level, integrated voltage regulators with embedded inductors, sub-THz passive components for 5G/6G applications, miniaturized RF wireless power transfer modules for IoT applications.
- Some of the developed technologies are transferred to Cadence, HPE, IBM and Intel.

DARPA Common Heterogeneous Integration and IP Reuse Strategies *Atlanta, GA, USA*
Graduate Research Assistant (PI: Madhavan Swaminathan) *Sep. 2017 - Aug. 2019*

- Investigated efficient method for electromagnetic modelling & optimization of interposer level interconnects and power delivery networks for heterogeneously integrated 2.5D systems.
- Developed a novel high-dimensional global optimization technique based on Additive Gaussian Processes, *Bayesian Optimization with Deep Partitioning Tree*, for chip-package co-optimization.
- Developed machine learning based co-analysis/optimization framework for integrated voltage regulators and embedded inductors.

Propagation Group, Georgia Tech *Atlanta, GA, USA*
Graduate Student Researcher (PI: Gregory David Durgin) *Aug. 2016 - Feb. 2017*

- Performed research on modelling, tuning and increasing operating range of ultra-low powered semi-passive backscattering communication using Quantum Tunneling RFID Tags.
- Assisted in developing models for characterizing gain of Quantum Tunneling RFID Tags.
- Performed kilometer range backscatter link measurements in midtown Atlanta to validate derived models.

Undergraduate Research, Bilkent University *Ankara, Turkey*
Researcher with focus on Antennas and Control Theory *Sep. 2014 - Jul. 2016*

- Designed, fabricated and performed low level programming of a universal control card for robotic platforms and demonstrated capabilities of developed card on a quadcopter and a land rover (industry/university collaboration)
- Designed & fabricated circular polarized antennas with increased bandwidth.
- Designed slotted sectoral waveguide arrays embedded in cylindrically stratified media using Taylor Tapering to limit Side Lobe Level.

Honors & Awards

April. 2019	**ECE Graduate Research Assistant Excellence Award** School of ECE, Georgia Tech	*Atlanta, GA*
Oct. 2018	**Best Student Paper Award** IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems	*San Jose, USA*
Nov. 2017	**2nd place Best Poster Award** Power Delivery for Electronic Systems Consortium (PDES), Georgia Tech	*Atlanta, USA*
May 2017	**1st place Best Poster Award** Power Delivery for Electronic Systems Consortium (PDES), Georgia Tech	*Atlanta, USA*
2016-2017	**Marion A. and Henry C. Bourne Fellowship** Offered at admission to PhD program by School of ECE, Georgia Tech	*Atlanta, USA*
2015-2016	**Tubitak Undergraduate Thesis Award** Bilkent University	*Ankara, Turkey*
2013-2016	**Excellence Scholarship** Bilkent University	*Ankara, Turkey*

Teaching & Professional Activities

Present	**Reviewer**, IEEE Access, IEEE TCPMT	*Atlanta, USA*
Spring '18, '19	**Teaching Assistant** Graduate level Microwave Design (ECE 6360), Georgia Tech	*Atlanta, USA*
2017-2018	**Opportunity Research Scholar Mentor** Research mentor of a team of undergraduate students	*Atlanta, USA*
Fall '16	**Teaching Assistant** Undergraduate level Circuit Analysis (ECE 2040), Georgia Tech	*Atlanta, USA*

Publications

Book Chapter

1. **H. M. Torun**, M. Larbi and M. Swaminathan, "Machine Learning based Optimization and Uncertainty Quantification for Integrated Systems", in Machine Learning in VLSI CAD, Springer, Editors: Ibrahim Elfadel, Duane Boning & Xin Li, 2019.

– The chapter covers how machine learning techniques can be used to perform optimization and uncertainty quantification in analog design layer of VLSI design hierarchy. The methods shown are demonstrated on System-in-Package integrated voltage regulators.

Journal Papers

1. M. Lee, A. Singh, **H. M. Torun**, J. Kim, S. Lim, M. Swaminathan, S. Mukhopadhyay, *"Automated I/O Library Generation for Interposer-based System-in-Package Integration of Multiple Heterogeneous Dies"*, IEEE Transactions on Components, Packaging and Manufacturing Technology (CPMT), under review.

2. S. Mukhopadhyay, Y. Long, C. S. Nair, B. H. DeProspo, **H. M. Torun**, M. Kathaperumal, V. Smet, B. Mudassar, D. Kim, S. Yalamanchili, M. Swaminathan, *"Heteregenous Integration for Artificial Intelligence: Challenges and Opportunities"*, IBM Journal of Research and Development, 2019.

3. **H. M. Torun**, M. Swaminathan, *"High Dimensional Global Optimization Method for High-Frequency Electronic Design"*, IEEE Transactions on Microwave Theory and Techniques, 2019.

4. C. A. Pardue, **H. M. Torun**, M. L. F. Bellaredj, M. Swaminathan, *"RF Near-Field Coupling System Using Reverse PDN and Considering Electromagnetic Effects"*, in IEEE Transactions on Electromagnetic Compatibility, 2019.

5. R. Trinchero, M. Larbi, **H. M. Torun**, F. G. Canavero and M. Swaminathan, "Machine Learning and Uncertainty Quantification for Surrogate Models of Integrated Devices With a Large Number of Parameters", in IEEE Access, 2018.

6. C. Pardue, M. Bellaredj, **H. M. Torun**, M. Swaminathan and A. K. Davis, *"RF Wireless Power Transfer using Integrated Inductor"*, IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018.

7. **H. M. Torun**, M. Swaminathan, A. K. Davis, M. L. F. Belladredj, *"A Bayesian based Global Optimization Algorithm and its Application to Integrated Systems"*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018.

8. F. Amato, **H. M. Torun** and G.D. Durgin, "RFID Backscattering in Long-Range Scenarios", IEEE Transactions on Wireless Communications, 2018.

Conference Papers

1. **H. M. Torun**, A. C. Durgun, K. Aygun, M. Swaminathan, *"Enforcing Causality and Passivity of Neural Network Models of Broadband S-Parameters"*, IEEE 28th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2019.

2. K. Roy, M. Ahadi, **H. M. Torun**, R. Trinchero, M. Swaminathan, *"Inverse Design of Transmission Lineswith Deep Learning"*, IEEE 28th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2019.

3. **H. M. Torun**, H. Yu, N. Dasari, V. C. K Chekuri, A. Singh, J. Kim, S. Lim, S. Mukhopadhyay, M. Swaminathan, *"A Spectral Convolutional Net for Co-Optimization of Embedded Inductors and Integrated Voltage Regulators"*, International Conference on Computer-Aided Design (ICCAD), 2019.

4. J. Kim, G. Murali, H. Park, E. Qin, H. Kwon, V. C. K. Chekuri, N. Dasari, A. Singh, M. Lee, **H. M. Torun**, K. Roy, M. Swaminathan, S. Mukhopadhyay, T. Krishna, S. Lim, *"Architecture, Chip, and Package Co-design Flow for 2.5D Integration of Reusable IP Chiplets"*, ACM Design Automation Conference (DAC), 2019.

5. **H. M. Torun**, N. Dasari, A. Singh, M. Lee, J. Kim, H. Park, H. Kwon, E. Qin, T. Krishna, S. Lim, S. Mukhopadhyay, M. Swaminathan, *"Design Space Exploration of Power Delivery in Heterogeneous Integration"*, Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.

6. J. Kim, E. Qin, H. Park, **H. M. Torun**, M. Swaminathan, T. Krishna, S. Lim, *"Enabling Heterogeneous IP Reuse with Interposer-based 2.5D ICs and Custom Interface Protocol"*, Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.

7. M. Lee, A. Singh, **H. M. Torun**, J. Kim, S. Lim, M. Swaminathan, S. Mukhopadhyay, *"Automated Generation of All-Digital I/O Library Cells for Multiple Dies in System-in-Package Integration"*, Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.

8. M. Lee, J. Kim, A. Singh, **H. M. Torun**, M. Swaminathan, S. Lim, S. Mukhopadhyay, *"On the design of energy-efficient I/O circuits for interposer-based 2.5D system-in-Package"*, IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2018.

9. **H. M. Torun**, J. A. Hejase, J. Tang, W. D. Becker and M. Swaminathan, *"Bayesian Active Learning for Uncertainty Quantification of High Speed Channel Signaling"*, IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2018. (**Best Student Paper Award**)

10. M. Lee, A. Singh, **H. M. Torun**, J. Kim, S. Lim, M. Swaminathan, and S. Mukhopadhyay, "Automated Generation of All-Digital I/O Library Cells for System-in-Package Integration of Multiple Dies", IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2018.

11. **H. M. Torun** and M. Swaminathan, "Bayesian Framework for Optimization of Electromagnetics Problems", 2018 International Workshop on Computing, Electromagnetics, and Machine Intelligence (CEMi), Stellenbosch, 2018.

12. K. Roy, **H. M. Torun** and M. Swaminathan, *"Preliminary Application of Deep Learning to Design Space Exploration"*, IEEE Electrical Design of Advanced Packaging & Systems Symposium, 2018.

13. **H. M. Torun**, M. Larbi and M. Swaminathan, *"A Bayesian Framework for Optimizing Interconnects in High-Speed Channels"*, IEEE MTT-S Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO), 2018.

14. M. Larbi, **H. M. Torun**, M. Swaminathan, I. S. Stievano, F. G. Canevero and P. Besnier *"Uncertainty Quantification of SiP based Integrated Voltage Regulator"*, 22nd IEEE Workshop on Signal and Power Integrity (SPI) 2018.

15. C. Pardue, **H. M. Torun**, M. Bellaredj and M. Swaminathan, *"System Level Efficiency Analysis for Regulated RF Near Field Coupling"*, IEEE MTT-S Wireless Power Transfer Conference (WPTC) 2018.

16. E. Lee, M. Amir, S. Sivapurapu, C. Pardue, **H. M. Torun**, M. Bellaredj, M. Swaminathan and S. Mukhopadyay *"A System-in-Package Based Energy Harvesting for IoT Devices with Integrated Voltage Regulators and Embedded Inductors"*, IEEE 68th Electron. Compon. Technol. Conf. (ECTC) 2018.

17. **H. M. Torun**, C. Pardue, M. L. F Belladredj, A. K. Davis and M. Swaminathan, *"Machine Learning Driven Advanced Packaging and System Miniaturization of IoT for Wireless Power Transfer Solutions"*, IEEE 68th Electron. Compon. Technol. Conf. (ECTC) 2018.

18. **H. M. Torun** and M. Swaminathan, *"A New Machine Learning Approach for Optimization and Tuning of Integrated Systems"*, DesignCon 2018.

19. **H. M. Torun** and M. Swaminathan, *"Black-Box Optimization of 3D Integrated Circuits using Machine Learning"*, IEEE 26th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), 2017.

20. **H. M. Torun** and M. Swaminathan, *"Black-Box Optimization of 3D Integrated Circuits"*, Computational Modelling of Multi-Uncertainty and Multi-Scale Problems (COMUS), September 2017.

21. F. Amato, **H. M. Torun**, and G. D. Durgin, "Beyond the Limits of Classic Backscattering Communications: a Quantum Tunneling RFID Tag," IEEE International Conference on RFID, 2017.

Skills

Laboratory Devices	Vector Network Analyzer, Spectrum Analyzer, Oscilloscope, Operations in Anechoic Chamber
EM Simulation Software	Ansys HFSS and Maxwell, CST Microwave Studio
RF Circuit & Layout Software	Keysight ADS, NI AWR Microwave Office, Cadence PowerSI
Software & Programming	Matlab, Python, PyTorch, C, GNU Radio

References

Prof. Madhavan Swaminathan
School of Electrical and Computer Engg.
Georgia Institute of Technology
Atlanta, GA, USA 30332-0250
madhavan.swaminathan@ece.gatech.edu
☎ (404)-385-6580

Wiren Dale Becker, PhD.
Chief Engineer of Electrical Packaging
IBM Systems
Poughkeepsie, NY, USA 12601
wbecker@us.ibm.com
☎ (845)-435-6735

Prof. Saibal Mukhopadhyay
School of Electrical and Computer Engg.
Georgia Institute of Technology
Atlanta, GA, USA 30332-0250
saibal.mukhopadhyay@ece.gatech.edu
☎ (404)-894-2688

Prof. Sung-Kyu Lim
School of Electrical and Computer Engg.
Georgia Institute of Technology
Atlanta, GA, USA 30332-0250
limsk@ece.gatech.edu
☎ (404)-894-0373