WANG, YI(EATHON)

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QUALIFICATION & CAREER OBJECTIVE

A PhD candidate with research background in machine learning techniques assisted design automation. Seeking an full time R&D position to increase data efficiency in business and deliver valuable products via data analytics and data driven methods.

EDUCATION

Ph.D. in Electrical Engineering Aug 2014 - Dec 2019(expected)
North Carolina State University (NCSU)

M.Sc. in Electrical Engineering Aug 2012 - Aug 2014
Thesis: Analog MPPT IC for Solar Cells, NCSU

B.S. in Electrical Engineering Sept 2008 - Jul 2012
University of Electronic Science and Technology of China, P.R. China

Deep Learning Course
Stanford CS229:Machine Learning; Stanford CS224n: Natural Language Processing with Deep Learning; Improving Deep Neural Networks: Hyperparameter tuning, Regularization and Optimization; Sequence Models; NCSU Computer Vision.

INDUSTRY EXPERIENCE

CAD Machine Learning Research & Development Intern, Analog Devices Inc.(ADI)
Wilmington, MA, Supervisor: David Smart May 2018 - Nov 2018

- System Design of Multi-Objective Surrogate Based Optimization Flow For Expensive Computational Experiments, including Bayesian and other types of optimization methods.
- System Design of Multi-Fidelity Surrogate Based Optimization Methodology Flow and its application on high speed interconnect EM Simulation acceleration.
- Low-sample high speed interconnect modelling through multiple machine learning techniques, including SVM, GP regression, Random Forest, etc.
- Generative Adversarial Network(GAN) on engineering inverse problem. Prototype model is implemented to generate SMART attributes of failed drive in large scale storage system.

Machine Learning Research & Development Intern, Hewlett Packard Enterprise(HPE)
Fremont, CA, Supervisor: Chris Cheng Jun 2017 - Aug 2017

- Investigated and implemented multiple machine learning modeling algorithms to predict large scale storage system drive failures and other unexpected events through Self-Monitoring and Report Technology(SMART)
- Investigated and implemented multiple parametric and non-parametric feature selection algorithms for feature engineering
- Delivered an fully automated code parser package for hard drive failure prediction

RESEARCH EXPERIENCE

Research Assistant, NSF Center for Advanced Electronics through Machine Learning (CAEML)
Raleigh, NC, Advisor: Professor Paul D. Franzon Jan 2017 - Present

· Analog/RF IC IP Redesign and Reuse Through Various Surrogate Based Machine Learning Methods

- Developed approach for Analog/RF IC design automation acceleration and explored the potential to reuse state of the art IP across different technology nodes

- Developed flow for accurate inductor model from electromagnetic(EM) simulation extraction and co-optimized with transistor level circuit. Demonstrated with VCO design.
- Developed flow for IP reuse and demonstrated with Mixer and Flip Flop design.

· Investigation on Machine Learning Algorithms to Profile and Optimize SerDes Circuit.

- Developed SerDes Behavioral Level Model and Optimized high level parameters through surrogate based machine learning method

Research Assistant, Microelectronics System Lab (MSL)
Raleigh, NC, Advisor: Professor Paul D. Franzon Aug 2014 - Dec 2016

· Multi-mode Interconnect Design Methodology and Implementation for High Density Links

- Investigated Multi-Mode signaling theory and its application to crosstalk noise cancellation in transceiver design and implemented Transistor Level Circuit (IBM 8RF Technology)

Research Assistant, NSF Future Renewable Electric Energy Delivery and Management System Center (FREEDM)
Raleigh, NC, Advisor: Professor Alex Q. Huang (UT Austin) Aug 2012 - Aug 2014

- Master Thesis: An Analog Maximum Power Point Tracking (MPPT) IC Design with Perturbation & Observation (P&O) and Fractional Open Circuit Voltage (FOCV) Control Methods for Solar Cells

NLP DEEP LEARNING RELATED PROJECT EXPERIENCE

Sentiment Analysis: Emojifier modelling

- Train Emojifier baseline model with method of averaging GloVe vector outputs and reach 84% accuracy; An advanced model leverages LSTM with an additional pretrained embedding layer using GloVe data with 87% accuracy for test set. Model is implemented with GloVe 50 dimension pretrained data and Keras.

Part of Speech tagging: Named-Entity Recognition using conditional random field

- Add feature functions to training dataset from CoNLL2002 Corpus available in NLTK and Train the model using Pycrfsuite with approximately 80% accuracy.

Speech Recognition: Trigger Word Detection

- Synthesize training audio clips by inserting positive and negative audio segments over background noise at random time step without overlapping. Test set has 25 clips of human saying sentences containing positive word and other random words. Model output is labeled as 1 for 50 consecutive time steps after positive words appearing in the clip. Model is trained with GRU with test accuracy of 94%.

RESEARCH PUBLICATIONS & PRESENTATIONS IN EDA

Y.Wang, P.D.Franzon "RFIC IP Redesign and Reuse Through Surrogate Based Machine Learning Method", *IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization for RF, Microwave, and Terahertz Applications (NEMO),* 2018

Y.Wang, P.D.Franzon "Efficient Analog/RF IP Optimization and Reuse via Machine Learning", *IEEE International Workshop on Design Automation for Analog and Mixed-Signal Circuit in International Conference On Computer Aided Design(ICCAD),* 2018

Y.Wang, P.D.Franzon, D.Smart, B.Swahn "Multi-Fidelity Surrogate based Optimization For Electromagnetic Simulation Acceleration", *IEEE International Conference On Computer Aided Design(ICCAD),* 2019 submitted

TECHIQUE SKILLS

- EDA Tools: Cadence Spectre; Synopsys Hspice & CosmosScope; Mentor Graphics Modelsim; Matlab Simulink
- Machine Learning Libraries & Frameworks: Numpy; Scipy; Pandas; Matplotlib; Scikit-Learn; Tensorflow; Keras; Surrogate Modelling (SUMO) Optimization toolbox
- Programming Languages: Python; Verilog; C; SKILL; MATLAB