Welcome to the Fall 2018 Semiannual Meeting

of the Center for Advanced Electronics through Machine Learning—CAEML. The students and faculty are excited to share their latest research findings with the center’s industry members.

Attendees at the Spring meeting told us that the student poster session was a highlight, and some recommended that it be made even longer. In response, the agenda for this meeting allocates over two hours for the poster session, and we have asked the currently supported faculty to deliver only very brief “quad chart reports” on their projects. During the poster session, you can delve into the technical details of the work with the graduate student researchers.

We have a very full agenda for this meeting. Two items are of highest priority, namely,

(i) Reports on currently funded projects: presentation of recent activities and research results, and
(ii) Presentation and review of newly proposed projects.

To ensure that there is sufficient time to review the current and proposed projects, attendees should anticipate that the daily schedule will be heavily micromanaged and, at times, that interesting discussions may be cut short. We trust that attendees will be amendable to continuing those discussions via web conference, email, or phone in the weeks following this face-to-face meeting. In particular, the directors wish to solicit the IAB’s input on a redesign of the CAEML website, new member recruitment, and topics for upcoming webinars, but we suspect we may not have the opportunity to fully explore all those topics over the next 1.5 days.

Finally, we want to remind the industry members that one of the best ways to enable technology transfer is through student summer internships at member companies. We encourage the industry representatives to talk with the students at this meeting about such opportunities. Afterward, you can find copies of the CAEML students’ resumes in the “members only” portion of the CAEML website.

Thank you for your support of our research.

Elyse Rosenbaum
Center Director, University of Illinois at Urbana-Champaign

Paul Franzon
Site Director, North Carolina State University

Madhavan Swaminathan
Site Director, Georgia Tech
AGENDA

Thursday, October 25, 2018
Klaus Advanced Computing Building Room 1116

7:45 AM  Registration, Breakfast, and Networking

8:30 AM  Welcoming Remarks | Madhavan Swaminathan, Georgia Tech CAEML Site Director; Steven McLaughlin, Dean, College of Engineering; Magnus Egerstedt, Chair School of Electrical and Computer Engineering; Eric Vogel, Deputy Director Institute for Electronics & Nanotechnology

8:50 AM  Introduction of attendees | Dale Becker, IAB Chair

9:05 AM  Presentation by Dee Hoffman, NSF IUCRC Assessment Coordinator

9:20 AM  State of Center Report | Elyse Rosenbaum, CAEML Director

9:35 AM  Closed door IAB meeting | Attendance restricted to IAB and NSF
1. Approval of previous meeting minutes
2. Election of Chair & Vice Chair for 2019-2021

10:05 AM  15 Minute COFFEE BREAK

PROGRESS REPORTS FOR PROJECTS IN FINAL YEAR OF FUNDING
[5 minute presentation, 5 minutes Q&A/LIFE forms]

B. Floyd and P. Franzon

10:30 AM  1A5 Progress Report: Behavioral Model Development for High-Speed Links
(10 minute presentation) M. Swaminathan, J. Schutt-Ainé and P. Franzon

10:45 AM  1A6 Progress Report: Models to Enable System-level Electrostatic Discharge Analysis
E. Rosenbaum

10:55 AM  1A7 Progress Report: Optimization of Power Delivery Networks for Maximizing Signal Integrity
C. Ji and M. Swaminathan

11:05 AM  2A6 Progress Report: Causal Inference for Early Detection of Hardware Failure
N. Kiyavash, M. Raginsky, E. Rosenbaum

11:15 AM  5 Minute BREAK

PROGRESS REPORTS & PROPOSALS FOR CONTINUING PROJECTS
[5 minute presentation, 5 minutes Q&A/LIFE forms]

A. Cangellaris and M. Raginsky

A. Raychowdhury & M. Swaminathan
AGENDA


12:00 PM LUNCH & Poster Session for Current Projects- 2 hrs. 20 min

2:20 PM LIFE Form completion for all current projects

NEW PROJECT PROPOSALS 20 minute presentation, 5 minutes Q&A, 5 minutes LIFE forms

2:40 PM Concurrent Graduate Student Meeting


4:10 PM COFFEE BREAK 10 min


5:50 PM 1st Day Wrap Up Meeting

Attendance restricted to Center Directors, IAB and NSF

6:15 PM DINNER at 5 Seasons Westside

Bus transportation provided to dinner and to hotels afterwards

Please note the 8:00 start on DayTwo. Breakfast will be available starting at 7:15.
AGENDA

Friday, October 26, 2018
Klaus Advanced Computing Building Room 1116

7:15 AM  Registration, Breakfast, and Networking

NEW PROJECT PROPOSALS  [20 minute presentation, 5 minutes Q&A, 5 minutes LIFE forms]

8:00 AM  New Project Proposal P18-8: ML for Board Level Analysis
          M. Swaminathan, E. Rosenbaum

8:30 AM  New Project Proposal P18-9: Expedient High-Speed Bus PCB Layout Analysis through
          Machine Learning  | X. Chen, J. Schutt-Ainé, A. Cangellaris

9:00 AM  New Project Proposal P18-10: Application of ML for Generating Interconnect Models with
          Predictive Capability | M. Swaminathan, J. Schutt-Ainé

9:30 AM  COFFEE BREAK  [Faculty respond to LIFE forms]

9:45 AM  New Project Proposal P18-11: Pseudo-Supervised Machine Learning for Broadband
          Macromodeling | J. Schutt-Ainé

10:15 AM New Project Proposal P18-12: Exploring Unknown Spaces for Component and System
         Level Modeling | S. Vasudevan

         through Machine Learning | A. Aysu, P. Franzon

11:15 AM New Project Proposal P18-16: Design Space Exploration using DNN
         M. Swaminathan, P. Franzon, R. Davis, E. Rosenbaum

11:45 AM LUNCH  [PIs respond to LIFE forms]

12:15 PM LIFE form review and discussion
          Led by D. Becker & D. Hoffman

1:15 PM  Discussions and voting for January 1, 2019 allocations
          Attendance restricted to NSF & IAB

3:00 PM  IAB Report out, Action items and plans for next meeting

3:30 PM  Adjourn
CAEML Semiannual Meeting • October 25 & 26, 2018

CAEML RESEARCH LEADERS

Aydin Aysu
https://www.ece.ncsu.edu/people/aaysu/

Aydin Aysu is currently an Assistant Professor in the Electrical and Computer Engineering Department and an Adjunct Professor at the Computer Science Department of North Carolina State University. Prior to joining NC State, he was a Post-Doctoral Research Fellow at the University of Texas at Austin from 2016 to 2018. He received his Ph.D. degree in Computer Engineering from Virginia Tech in 2016. He received his M.S. degree in Electronics Engineering and B.S. degree in Microelectronics Engineering from Sabanci University, Istanbul, Turkey, respectively in 2010 and 2008.

Dr. Aysu’s research focuses on the development of secure systems that prevent cyberattacks targeting hardware vulnerabilities. To this end, his research interests lie at the intersection of applied cryptography, digital hardware design, and computer architectures. He currently co-chairs the security track at the IEEE International Conference on Reconfigurable Computing and FPGAs, and he is a guest editor for the special issue “Post-Quantum Cryptography: From Theoretical Foundations to Practical Deployments” of the MDPI Journal of Cryptography.

Dror Baron
ece.ncsu.edu/people/dzbaron

Dror Baron received the B.Sc. (summa cum laude) and M.Sc. degrees from the Technion - Israel Institute of Technology, Haifa, Israel, in 1997 and 1999, and the Ph.D. degree from the University of Illinois at Urbana-Champaign in 2003, all in electrical engineering. From 1997 to 1999, he was a Modem Designer at Witcom Ltd. From 1999 to 2003, he was a Research Assistant at the University of Illinois at Urbana-Champaign, where he was also a Visiting Assistant Professor in 2003. From 2003 to 2006, he was a Postdoctoral Research Associate in the Department of Electrical and Computer Engineering at Rice University, Houston, TX. From 2007 to 2008, he was a Quantitative Financial Analyst with Menta Capital, San Francisco, CA. From 2008 to 2010 he was a Visiting Scientist in the Electrical Engineering Department at the Technion. Dr. Baron joined the Department of Electrical and Computer Engineering at North Carolina State University in 2010, and is currently an associate professor. His research interests include information theory and statistical signal processing.

Andreas Cangellaris
ece.illinois.edu/directory/profile/cangella

Dr. Cangellaris is the Vice Chancellor for Academic Affairs and Provost and M.E. VanValkenburg Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. He earned his M.S. and Ph.D. degrees in Electrical Engineering at the University of California, Berkeley, in 1983 and 1985, respectively. From 2013-2017 Cangellaris was the Dean of the College of Engineering and prior to that served as Head of the Department of Electrical and Computer Engineering.

He is broadly recognized for his research in applied and computational electromagnetics and applications to the signal integrity of integrated electronic circuits and systems. His research has produced several design methods and computer tools that are used widely in the microelectronics industry. He has written or co-written more than 250 papers. He joined the faculty at Illinois in 1997. He was an Associate Provost Fellow on the Urbana campus from 2006 to 2008. He is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), and the recipient of a Humboldt Foundation Research Award, the U.S. Army Research Laboratory Director’s Coin, and the IEEE Microwave Theory & Techniques Distinguished Educator Award.
Xu Chen  
https://ece.illinois.edu/directory/profile/xuchen1

Dr. Chen received his B.S., M.S., and Ph.D. degrees, all in Electrical Engineering, from the University of Illinois Urbana-Champaign in 2005, 2014, and 2018. He is currently a Teaching Assistant Professor at the Department of Electrical and Computer Engineering at the University of Illinois Urbana-Champaign. His research interests are in stochastic modeling for electromagnetics and circuits, computer-aided design, uncertainty quantification, and machine learning.

From 2005 to 2012, he was an engineer with IBM in Poughkeepsie, NY. He has also worked at Electronic Design Automation group at Apple. He is a recipient of the IEEE EDAPS Best Symposium Paper Award in 2017, and was also a recipient of the Raj Mittra Outstanding Research Award, Mavis Future Faculty Fellowship, Harold L. Oleson Award, and Ernest A. Reid Fellowship Award. He is a member of IEEE and SIAM.

Rhett Davis  
ece.ncsu.edu/people/wdavis

W. Rhett Davis is a Professor of Electrical and Computer Engineering at North Carolina State University. He received B.S. degrees in electrical engineering and computer engineering from North Carolina State University, Raleigh, in 1994 and M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley in 1997 and 2002, respectively. He received the National Science Foundation’s Faculty Early Career Development (CAREER) award in 2007, and received the Distinguished Service Award from the Silicon Integration Initiative (Si2) in 2012 for his research in the development of standards for electronic design automation (EDA) and his development of the FreePDK open-source, predictive process design kit. He is working with Si2 to develop standards for system-level power modeling and compact modeling of device reliability. He has been an IEEE member since 1993 and a Senior Member since 2011. He has published over 50 scholarly journal and conference articles. He has worked at Hewlett-Packard (now Keysight) in Boeblingen, Germany and consulted for Chameleon Systems, Qualcomm, BEECube, and Silicon Cloud International. Dr. Davis’s research is centered on electronic design automation for integrated systems in emerging technologies. He is best known for his efforts in design enablement, 3DIC design, thermal analysis, circuit simulation, and power modeling for systems-on-chip and chip multiprocessors.

Brian Floyd  
people.engr.ncsu.edu/bafloyd

Brian Floyd received the B.S. with highest honors, M. Eng., and Ph.D. degrees in electrical and computer engineering from the University of Florida, Gainesville in 1996, 1998, and 2001, respectively. From 2001 to 2009, he worked at the IBM T. J. Watson Research Center in Yorktown Heights, New York, first as a research staff member and then later as the manager of the millimeter-wave circuits and systems group. His work at IBM included the development of silicon-based millimeter-wave transceivers, phased arrays, and antenna-in-package solutions. In 2010, Dr. Floyd joined the Department of Electrical and Computer Engineering at North Carolina State University as an Associate Professor. His research interests include RF and millimeter-wave circuits and systems for communications, radar, and imaging applications.

Dr. Floyd has authored or co-authored over 90 technical papers and has 25 issued patents. He currently serves on both the steering and technical program committees for the IEEE RFIC Symposium. From 2006 to 2009, he served on the technical advisory board of the Semiconductor Research Corporation (SRC) integrated circuits and systems science area, and currently serves as a thrust leader for the SRC’s Texas Analog Center of Excellence. He received the 2016 NC State Outstanding Teacher Award, the 2015 NC State Chancellor’s Innovation Award, the 2014 IBM Faculty Award, the 2011 DARPA Young Faculty Award, the 2004 and 2006 IEEE Lewis Winner Awards for best paper at the International Solid-State Circuits Conference, and the 2006 and 2011 Pat Goldberg Memorial Awards for the best paper within IBM Research.
Paul Franzon  
*ece.ncsu.edu/erl/faculty/paulf*  
Paul D. Franzon is currently a Cirrus Logic Distinguished Professor of Electrical and Computer Engineering and Director of Graduate Programs at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Australia.  
He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom, and three companies he cofounded: Communica, LightSpin Technologies, and Polymer Braille Inc. His current interests center on the technology and design of complex microsystems incorporating VLSI, MEMS, advanced packaging, and nano-electronics. He has led several major efforts and published over 300 papers in those areas. In 1993, he received an NSF Young Investigators Award; in 2001, he was selected to join the NCSU Academy of Outstanding Teachers; and in 2003, he was named an Alumni Undergraduate Distinguished Professor. He received the Alcoa Research Award in 2005, and the Board of Governors Teaching Award in 2014. He served with the Australian Army Reserve for 13 years as an Infantry Soldier and Officer. He is a Fellow of the IEEE.

Chuanyi Ji  
*jic.ece.gatech.edu*  
Chuanyi Ji’s research is in large-scale networks, machine learning, and big data sets. She received a B.S. degree from Tsinghua University, Beijing, China, in 1983, an M.S. degree from the University of Pennsylvania, Philadelphia in 1986, and a Ph.D. degree from the California Institute of Technology, Pasadena in 1992, all in Electrical Engineering. She was an Assistant and Associate Professor from 1991 to 2001 at the Rensselaer Polytechnic Institute (RPI), Troy, NY. She was a visitor/consultant at Bell Labs Lucent, Murray Hill, NJ in 1999, and a visiting faculty member at the Massachusetts Institute of Technology, Cambridge in 2000. She is an Associate Professor with the Georgia Institute of Technology, Atlanta, which she joined in 2001. Dr. Ji’s awards include a CAREER award from NSF and an Early CAREER award from RPI. She was a co-founder of a startup company on network monitoring and management.

Negar Kiyavash  
https://www.ece.gatech.edu/faculty-staff-directory/negar-kiyavash  
Negar Kiyavash is a joint Associate Professor in the H. Milton Stewart School of Industrial & Systems Engineering (ISyE) and the School of Electrical and Computer Engineering (ECE) at Georgia Institute of Technology (Gatech). Prior to joining Gatech, she was a Willett Faculty Scholar and a joint Associate Professor of Industrial and Enterprise Engineering (IE) and Electrical and Computer Engineering (ECE) at the University of Illinois. Her research interests are in design and analysis of algorithms for network inference and security. She is a recipient of NSF CAREER and AFOSR YIP awards and the Illinois College of Engineering Dean’s Award for Excellence in Research.

Sung-Kyu Lim  
*ece.gatech.edu/faculty-staff-directory/sung-kyu-lim*  
Sung Kyu Lim received the B.S., M.S., and Ph.D. degrees from the University of California at Los Angeles in 1994, 1997, and 2000, respectively. He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology in 2001, where he is currently Dan Fielder Endowed Chair Professor. His current research interests include modeling, architecture, and electronic design automation (EDA) for 3D ICs. His research on 3D IC reliability is featured as Research Highlight in the Communication of the ACM in 2014. His 3D IC test chip published in the IEEE International Solid-State Circuits Conference (2012) is generally considered the first multi-core 3D processor ever developed in academia. Dr. Lim is a recipient of the National Science Foundation Faculty Early Career Development (CAREER) Award in 2006. He received the Best Paper Awards from the IEEE Asian Test Symposium (2012) and the IEEE International Interconnect Technology Conference (2014). He has been an Associate Editor of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) since 2013. He received the Class of 1940 Course Survey Teaching Effectiveness Award from Georgia Institute of Technology (2016).
Maxim Raginsky

csl.illinois.edu/directory/faculty/maxim

Maxim Raginsky received B.S. and M.S. degrees in 2000 and a Ph.D. degree in 2002 from Northwestern University, all in Electrical Engineering. He has held research positions with Northwestern, the University of Illinois at Urbana-Champaign (where he was a Beckman Foundation Fellow from 2004 to 2007), and Duke University. In 2012, he returned to UIUC, where he is currently an Associate Professor and William L. Everett Fellow with the Department of Electrical and Computer Engineering, and a member of the Decision and Control Group in the Coordinated Science Laboratory. His research interests include understanding, modeling, and analyzing complex systems that have capabilities for sensing, communication, adaptation, and decision-making and that can operate effectively in uncertain and dynamic environments. His research examines new angles and perspectives between machine learning, control, optimization, and information theory.

Arijit Raychowdhury

ece.gatech.edu/faculty-staff-directory/arijit-raychowdhury

Arijit Raychowdhury (M-'07, SM-'13) is currently an Associate Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology where he currently holds the ON Semiconductor Junior Research Professorship. He received his Ph.D. degree in Electrical and Computer Engineering from Purdue University and his B.E. in Electrical and Telecommunication Engineering from Jadavpur University, India. He joined Georgia Tech in January, 2013. His industry experience includes five years as a Staff Scientist in the Circuits Research Lab, Intel Corporation and a year as an Analog Circuit Designer with Texas Instruments Inc. His research interests include digital and mixed-signal circuit design, design of on-chip sensors, memory, and device-circuit interactions. Dr. Raychowdhury holds more than 25 U.S. and international patents and has published over 100 articles in journals and refereed conferences. He is the winner of the NSF CRII Award, 2015; Intel Labs Technical Contribution Award, 2011; Dimitris N. Chorafas Award for outstanding doctoral research, 2007; the Best Thesis Award, College of Engineering, Purdue University, 2007; Best Paper Awards at the International Symposium on Low Power Electronic Design (ISLPED) 2012, 2006; IEEE Nanotechnology Conference, 2003; SRC Technical Excellence Award, 2005; Intel Foundation Fellowship 2006, NASA INAC Fellowship 2004, and the Meissner Fellowship 2002. Dr. Raychowdhury is a Senior Member of the IEEE.

Elyse Rosenbaum

eyse.ece.illinois.edu

Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. She received the B.S. degree (with distinction) from Cornell University in 1984, the M.S. degree from Stanford University in 1985, and the Ph.D. degree from the University of California, Berkeley in 1992, all in electrical engineering. From 1984 through 1987, she was a Member of Technical Staff at AT&T Bell Laboratories in Holmdel, NJ.

Dr. Rosenbaum’s present research interests include component and system-level ESD reliability, ESD-robust high-speed I/O circuit design, compact modeling, mitigation strategies for ESD-induced soft failures, and machine-learning aided behavioral modeling of microelectronic components and systems. She has authored nearly 200 technical papers. From 2001 through 2011, she was an editor for IEEE Transactions on Device and Materials Reliability. She is currently an editor for IEEE Transactions on Electron Devices. Dr. Rosenbaum was the General Chair for the 2018 International Reliability Physics Symposium.

Dr. Rosenbaum was the recipient of a Best Student Paper Award from the IEDM, as well as Outstanding and Best Paper Awards from the EOS/ESD Symposium. She has received an NSF CAREER award, an IBM Faculty Award, and the ESD Association’s Industry Pioneer Recognition Award. Dr. Rosenbaum is a Fellow of the IEEE.
José Schutt-Ainé

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José E. Schutt-Ainé received a B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC) in 1984 and 1988, respectively. He was an Application Engineer at the Hewlett-Packard Technology Center, Santa Rosa, CA, where he was involved in research on microwave transistors and high-frequency circuits. In 1983, he joined UIUC, and then joined the Electrical and Computer Engineering Department and became a member of the Electromagnetics and Coordinated Science Laboratories. He is a consultant for several corporations. His current research interests include the study of signal integrity and the generation of computer-aided design tools for high-speed digital systems. Dr. Schutt-Ainé is the recipient of several research awards, including the 1991 National Science Foundation (NSF) MRI Award, the National Aeronautics and Space Administration Faculty Award for Research (1992), the NSF MCAA Award (1996), and a UIUC National Center for Supercomputing Applications Faculty Fellow Award (2000). He is an IEEE Fellow and is currently serving as Co-Editor-in-Chief of the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT).

Madhavan Swaminathan
c3ps.gatech.edu; epsilonlab.ece.gatech.edu

Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE) and Director of the Center for Co-Design of Chip, Package, System (C3PS), Georgia Tech. He formerly held the position of Joseph M. Pettit Professor in Electronics in ECE and Deputy Director of the NSF Microsystems Packaging Research Center, Georgia Tech. Prior to joining Georgia Tech, he was with IBM working on packaging for supercomputers. He is the author of 450+ refereed technical publications, holds 29 patents, is primary author and co-editor of 3 books, and was founder and co-founder of two start-up companies (E-System Design and Jacket Micro Devices) and founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the CPMT society on Signal Integrity in the Asian Region. He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE EMC society. He received his M.S. and Ph.D. degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.

Shobha Vasudevan
https://ece.illinois.edu/directory/profile/shobhav

Shobha Vasudevan is an associate professor in the departments of Electrical and Computer Engineering and Computer Science at the University of Illinois at Urbana-Champaign. Her research interests span embedded systems and algorithms. In embedded systems, she works on verification, reliability and security; she is currently working on these for autonomous vehicles.

She likes to think about non-convex and functional optimization, large scale graph search, and machine learning based algorithms. She has applied these algorithms to analyze biological knowledge networks, enterprise log data for security intrusions, and patient health monitoring data.

She has won the Best Paper Award in DAC 2014, NSF CAREER award, the ACM SIGDA outstanding new faculty award, the Dean’s Award for Excellence in Research, Best paper award in VLSI Design 2014, IEEE Council of EDA Early Career Award, a UIUC award for mentoring women in engineering and several best paper nominations. GoldMine, a verification software from her group has been developed into a commercial product since 2014 and licensed by multiple semiconductor and electronic design automation companies from UIUC.
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<th>Project ID</th>
<th>Project Title</th>
<th>Project PIs</th>
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<td>Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems</td>
<td>Raginsky, Cangellaris</td>
<td>3 years</td>
<td>Jan 1 2017</td>
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<td>Causal Inference for Early Detection of Hardware Failure</td>
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<td>Applying Machine Learning to Back End IC Design</td>
<td>Davis, Franzon, Baron</td>
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*allowed extension to finish spending allocated funds past end date of sub-award
## Project Summary

**Title:** Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems  
**Date:** 9/1/17

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**Center:** Center for Advanced Electronics through Machine Learning (CAEML)  
**Tracking No.:** 1A1  
**Project Leader(s):** Maxim Raginsky (UIUC) and Andreas Cangellaris (UIUC)  
**Phone(s):** (217) 244-1782  
**E-mail(s):** maxim@illinois.edu, cangella@illinois.edu  
**Proposed Budget:** $96k  
**Type:** Continuing  
**Other Faculty Collaborator(s):** Chuanyi Ji (Georgia Tech)

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### Project Description:

The project focuses on theoretical foundations and modular algorithmic solutions for ML-driven design, simulation, and verification of high-complexity, multifunctional electronic systems. Behavioral system modeling provides a systematic approach to reconciling the variety of physics-based and simulation-based models, expert knowledge, and other possible means of component description commonly introduced in electronic systems modeling. In complex electronic systems, each component model comes with its own sources of errors, uncertainty, and variability, and the same applies to the way components and subsystems are connected and interact with each other in the integrated system. The modularity offered by the behavioral approach will be leveraged to develop mathematical tools for assessing the performance and minimal data requirements for learning a low-complexity representation of the system behavior, one component or subsystem at a time, from measured and simulated data even in highly complex and uncertain settings. We will develop and implement the full ML algorithmic pipeline and quantify its end-to-end performance in applications pertinent to multifunctional electronic system design, simulation, and verification.

### Progress to Date (if applicable):

1. Analyzed local and global stability of gradient descent with backpropagation, the standard method for training complex nonlinear models, such as neural networks.  
2. Developed methodology for learning stable recurrent neural network models that compose well with circuit simulators.  
3. Developed methodology for integrating flexible probabilistic generative models into passive macromodeling pipeline.

### Experimental plan (current year only):

In the context of behavioral system modeling, both learning algorithms and their outputs are probabilistic programs that consist of deterministic transformations (nominal device models), random variable generators (to capture noise and component/process variability), and probabilistic conditioning (to capture constraints or relations among internal and external variables). Furthermore, significant structural complexity of realistic electronic systems leads to chaotic behavior of the electromagnetic fields responsible for EMI events. As such, in addition to often being computationally prohibitive, a deterministic approach to computer-aided investigation of performance tradeoffs may not be sufficient to inform design decisions. The use of probabilistic program formalism will allow us to develop robust and mathematically sound techniques for capturing all sources of noise and variability in behavioral models and for quantifying the concentration of typical system behavior around the mean or median nominal model. In addition, it will pave the way for more efficient and meaningful predictive EMI analysis at the system level.

### Related work elsewhere and how this project differs:

To date, behavioral modeling of electronic systems in the presence of uncertainty/variability is dominated by approaches that propagate the stochastic attributes of any input parameters to the output. In contrast, our method will produce a low-complexity representation of the system behavior from measured and simulated data that lends itself to expedient, yet accurate simulation.

### Proposed milestones for the current year:

1. Theoretical and algorithmic framework for modular ML.  
2. Identify test structure for system-level EMI modeling.

### Proposed deliverables for the current year:

1. Design and characterization of each element of the ML pipeline as a probabilistic program, including tools for uncertainty quantification in behavioral models.  
2. Report on the application of probabilistic modeling to expedite EMI modeling and simulation of realistic electronic systems.

### Potential Member Company Benefits:

System designers are confronting increasing demands on end-to-end system functionality integration and resilience, while facing competitive time-to-market and low-cost constraints. The increased complexity of these systems hinders high-fidelity predictive modeling and performance simulation, which, in turn, may lead to overly conservative designs that unnecessarily sacrifice performance and even increase cost. This project will tackle these pressing industry challenges.

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**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/18
<table>
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<tr>
<th>Project Summary</th>
<th>Title: Intellectual Property Reuse Through Machine Learning</th>
<th>Date: 9/1/17</th>
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<tr>
<td><strong>Center:</strong></td>
<td>Center for Advanced Electronics through Machine Learning (CAEML)</td>
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<tr>
<td><strong>Tracking No.:</strong></td>
<td>1A2</td>
<td><strong>Project Leader(s):</strong></td>
</tr>
<tr>
<td><strong>Phone(s):</strong></td>
<td>(919) 515-7351</td>
<td><strong>E-mail(s):</strong></td>
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<tr>
<td><strong>Other Faculty Collaborator(s):</strong></td>
<td>Baron (NCSU)</td>
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**Project Description:** The objective of this project was to demonstrate that machine learning can be applied to the problem of recasting an analog or full custom digital design from one technology node to another, assuming the same circuit topology.

**Progress to Date (if applicable):** A Bayesian optimization framework was put together to tackle this problem. It builds a coarse surrogate model of the design and then conducts screening on the design in order to reduce the number of design dimensions. Bayesian optimization is then used to find the optimal point in the new technology with the minimum number of iterations. A webinar was given on the tool and the underlying methods in August 2017. To date the tool has been demonstrated on a Balun and power amplifier circuit. The resulting designs were better than the human generated ones.

**Experimental plan (current year only):** We will demonstrate the design on a mixer and a serdes receiver. The receiver includes PLL, CTLE and DFE stages. As well as demonstrating the tool on each of the stages, we will demonstrate a new capability that considers tradeoff between the stages. This will be done using the surrogate models for the different stages together in an optimization tradeoff analysis. Different optimization strategies will be investigated. In addition, we will complete the measurement comparisons on the RF circuit blocks.

**Related work elsewhere and how this project differs:** Not aware of directly related work.

**Proposed milestones for the current year:** (1) Completion of Mixer design; (2) Design comparison with measurement; (3) Investigation for optimization of individual blocks in SerDes; (4) Investigation of co-optimization of blocks in SerDes.

**Proposed deliverables for the current year:** Demonstration and reports associated with these milestones. The tool has already been delivered to the Center for member distribution.

**Projected deliverables for Year 2 (if applicable):**

**Potential Member Company Benefits:** Improved ability to achieve optimal designs for analog and full custom blocks with a fixed circuit topology across different circuit nodes.

**Estimated Start Date:** 1/1/18  **Estimated Project Completion Date:** 12/31/18
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<tr>
<th><strong>Project Summary</strong></th>
<th><strong>Title:</strong> Behavioral Model Development for High-Speed Links</th>
<th><strong>Date:</strong> 9/1/17</th>
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<td><strong>Project Leader(s):</strong></td>
<td>Madhavan Swaminathan (GT), José Schutt-Ainé (UIUC), and Prof. Paul Franzon (NCSU)</td>
<td><strong>Project Leader(s):</strong></td>
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<td><strong>Phone(s):</strong></td>
<td>(404) 227-0087</td>
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<tr>
<td><strong>E-mail(s):</strong></td>
<td><a href="mailto:madhavan@ece.gatech.edu">madhavan@ece.gatech.edu</a>; <a href="mailto:josec@emlab.illinois.edu">josec@emlab.illinois.edu</a>; <a href="mailto:paulf@ncsu.edu">paulf@ncsu.edu</a></td>
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<td><strong>Other Faculty Collaborator(s):</strong></td>
<td>Chuanyi Ji (GT) and Maxim Raginsky (UIUC)</td>
<td><strong>Other Faculty Collaborator(s):</strong></td>
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**Project Description:** High-speed links consist of driver and receiver circuits connected to through interconnections in the chip, package, and printed circuit board. Over several decades, as the speed of the channel has increased, the driver and receiver circuits have become quite complex to compensate for any shortcomings of the channel; e.g., they contain pre-distortion, pre-emphasis, adaptive control, and equalization circuitry. This project’s goal is to apply machine-learning methods to systematically develop a hierarchy of behavioral models of circuits that have the same accuracy as the transistor-level models, but require 25–50X less CPU time and memory. The behavioral models will be suitably parameterized to include a range of channel conditions that can be used for design verification and optimization. Three approaches will be used: 1) using time domain data, 2) using X-parameters, and 3) building receiver models using system identification and surrogate modeling. We will compare the three approaches as part of this project.

**Progress to Date (if applicable):** We have developed behavioral models for fixed frequency oscillators and VCOs using neural networks (~10X faster than transistor models), based on collaboration with Cadence. This has resulted in an accepted paper at DATE ’17 conference. We are currently collaborating with Qualcomm on behavioral modeling of I/O drivers using RNN and with IBM on HSSCDR modeling. We have completed volterra kernel (VK) extraction using a second-order approximation. This extraction can be performed from harmonic balance (HB) simulation or using X parameters. This work has led to a paper that will be presented at the RADIO-17 conference. Using higher orders will necessitate a tensor representation to handle the large amount of X-parameter data. The data and algorithm will be used to train an ANN and automate the kernel generation process. For receiver modeling, the main outcome to date has been the identification of the Neural Network ARMAX modeling technique as one that gives high predictive accuracy for RXs using DFE and CTLE.

**Experimental plan (current year only):** Behavioral Modeling using Time Domain Data: The waveforms for training will be obtained from simulation (or measurement) of the transistor-level circuits. 1) Georgia Tech students have received training to use IBM’s HSSCDR tool where concepts and notations of high-speed channel design as well as syntax of HSSCDR tool have been presented for generating channels with different interconnect characteristics with emphasis on insertion loss, crosstalk, optimal equalization settings and analysis of eye diagrams. Data generated from this tool will be used for generating time-domain channel response using input-output waveforms and s-parameters. 2) We will explore algorithms that minimize the number of training data sets required by incorporating expert ML methods that can lead to automation for the generation of the training data sets where RNN based methods will be investigated. Behavioral Modeling using X-Parameter Data: Our efforts will focus on evaluating and validating the second-order VK. The device under test will be a buffer of CMOS type. X-parameter data will be obtained (a) from harmonic balance simulation using ADS and (b) from measurement using a nonlinear vector network analyzer (NVNA). The data obtained will be used to train an ANN into generating the kernels. We plan to demonstrate a prototype of this neuro-VK based simulation tool for a high-speed link driver and comparing the results with those of traditional IBIS simulations. Receiver Modeling: Demonstration of ability to model a measured receiver and a simulated one. Delivery of code that could be ported to an oscilloscope. Methods will be investigated to classify system noise so the impact of PSIJ can be predicted.

**Related work elsewhere and how this project differs:** This is based on earlier work the investigators did in the area of recurrent neural networks, identification modeling, surrogate modeling, and X-parameters. Opportunities exist to enable a high degree of automation in the model development process because of the advancements in ML algorithms.

**Proposed milestones for the current year:** Perform benchmark test with IBIS (Volterra); Software that uses machine learning for the generation of behavioral models for circuits used in high-speed signaling; Comparison of results for accuracy and speed (transistor circuits and IBIS); Implement x2ibus; Merge x2ibus and ML-Volterra methods; Automated software for behavioral model and SPICE netlist generation; Comparison of ML-based methods along with documentation for model development; Technology transfer through internships.

**Proposed deliverables for the current year:** Software that automates the behavioral model construction and SPICE netlist generation. Application to high-speed channels with 10–20 ports. Demonstration of 25X–50X speed-up. Predict transient voltage and currents at input and output of simulator. Complete RX modeling extraction. Comparison between the methods developed for determining best technique for a class of circuitry.

**Potential Member Company Benefits:** Accurate SPICE models with 25–50X reduction in simulation time.

**Estimated Start Date:** 1/1/18 **Estimated Project Completion Date:** Dec. 31, 2018
### Project Summary

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<th>Center:</th>
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<td>Project Leader(s):</td>
<td>Elyse Rosenbaum (UIUC); Maxim Raginsky (UIUC)</td>
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<td>Phone(s):</td>
<td>(217) 333-6754</td>
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<td><a href="mailto:elyse@illinois.edu">elyse@illinois.edu</a> <a href="mailto:maxim@illinois.edu">maxim@illinois.edu</a></td>
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<td>Madhavan Swaminathan (GT)</td>
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### Project Description

**Title:** Models to Enable System-level Electrostatic Discharge Analysis

The following have been developed. (1) I-V models for I/O pins that are relevant at ESD current levels under both power-on and power-off conditions; these multi-port models capture the multitude of current return paths. (2) RNN models for transient simulation of I/O pin response to ESD. By construction, the RNN model accurately represents the thermal equilibrium condition. The loss function used during training is designed to penalize unstable solutions. The RNN is implemented in Verilog-A and may be used in a variable time-step simulation. (3) Generative model for air discharge waveforms: \( P(X_1, X_2, Y_1, Y_2, Y_3) \), where \( X_1 \) is pre-charge voltage of the ESD source, \( X_2 \) is the speed at which the source approaches the equipment under test (EUT), \( Y_1 \) is the peak ESD current, \( Y_2 \) is the ESD pulse risetime, and \( Y_3 \) is the total charge transferred to the EUT. Bayesian inference is used to approximate the posterior distribution function; kernel density estimation is used to obtain the prior and likelihood distributions.

### Progress to Date

The following have been developed. (1) I-V models for I/O pins that are relevant at ESD current levels under both power-on and power-off conditions; these multi-port models capture the multitude of current return paths. (2) RNN models for transient simulation of I/O pin response to ESD. By construction, the RNN model accurately represents the thermal equilibrium condition. The loss function used during training is designed to penalize unstable solutions. The RNN is implemented in Verilog-A and may be used in a variable time-step simulation. (3) Generative model for air discharge waveforms: \( P(X_1, X_2, Y_1, Y_2, Y_3) \), where \( X_1 \) is pre-charge voltage of the ESD source, \( X_2 \) is the speed at which the source approaches the equipment under test (EUT), \( Y_1 \) is the peak ESD current, \( Y_2 \) is the ESD pulse risetime, and \( Y_3 \) is the total charge transferred to the EUT. Bayesian inference is used to approximate the posterior distribution function; kernel density estimation is used to obtain the prior and likelihood distributions.

### Experimental plan (current year only)

Benchmark 4 ESD simulation approaches against measurement data: circuit simulation vs. hybrid EM-circuit simulation; RNN transient models of the components vs. I-V models. Evaluate the feasibility of a more complex return-path model. Presently, all pins within a single net are lumped together for computational efficiency. Separating these pins would allow one to simulate noise coupling inside the package, which is a significant cause of ESD-induced soft-failures. Include additional features (inputs) in the generative model for air discharge; these features should describe the physical design of the EUT, e.g. its dimensions. Improve the dynamic range of the RNN circuit model (making it suitable for AC as well as transient simulations) by using additional inputs during training. Explore other applications of the models developed in this project. RNN models of circuits used in mixed-signal systems will be implemented using Verilog-AMS; the model accuracy and efficiency will be compared to behavioral models used more typically.

### Related work elsewhere and how this project differs

This project uniquely utilizes generative modeling to represent ESD events that are inherently stochastic in nature.

### Proposed milestones for the current year

(1) Quantify RNN complexity in terms of the (i) number of ports for the circuit being modeled and (ii) number of nodes in the circuit being modeled (if known). (2) Benchmark simulated waveforms against those obtained from measurement. (3) Demonstrate soft failure prediction capability. (4) Implement RNN circuit models using Verilog-AMS and benchmark the simulation results against other behavioral models.

### Proposed deliverables for the current year

(1) Code (python or Matlab) to learn models from data: multi-port I-V model of I/O pin ESD response, and generative model for air discharge. (2) RNN models with enhanced dynamic range.

### Potential Member Company Benefits

Provide a time-saving and cost-effective alternative to a hardware-based trial-and-error method to achieve system ESD robustness. The same RNN structure used for ESD response modeling can be used to obtain behavioral models needed for mixed-signal simulation of circuits and systems.

### Estimated Start Date

1/1/18

### Estimated Project Completion Date

12/31/18
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<th>Project Summary</th>
<th>Title: Optimization of Power Delivery Networks for Maximizing Signal Integrity</th>
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<td><strong>Project Leader(s):</strong></td>
<td>Madhavan Swaminathan and Chuanyi Ji (GT)</td>
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<tr>
<td><strong>Phone(s):</strong></td>
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<td><a href="mailto:madhavan@ece.gatech.edu">madhavan@ece.gatech.edu</a>, <a href="mailto:jichuanyi@gatech.edu">jichuanyi@gatech.edu</a></td>
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<td><strong>Other Faculty Collaborator(s):</strong></td>
<td>Elyse Rosenbaum, Maxim Raginsky, and Andreas Cangellaris (UIUC)</td>
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**Project Description:** Power distribution is a system-level problem in which the contributions from the chip, package, and printed circuit board are equally important. This, when combined with signal lines, can lead to models that can take a long time to simulate. With optimization being an integral part of design, co-optimization of the signal and power delivery network becomes necessary. As the number of control parameters increases, the co-optimization process can be very time-consuming. In addition, accounting for uncertainty of parameters and variation for complex systems can be challenging. The objective of this project is to explore and develop machine learning (ML) based software to optimize the system output response based on a large set of control parameters and compute BER of channels. We will focus on four applications: 1) 3D ICs; 2) Integrated Voltage Regulators (IVR); 3) Wireless Power Transfer (WPT) for IoT and 4) HSSCDR.

**Progress to Date (if applicable):** We have developed an EDA oriented Bayesian Optimization (BO) algorithm called Two-Stage Bayesian Optimization (TSBO) that has outperformed conventional ML & non-ML optimization algorithms. These have been applied to 1) Clock skew minimization of 3D ICs where TSBO resulted in 4.7% and 2.3% improvement in clock skew and temperature gradient with 4X faster convergence; 2) Multi-objective optimization of IVR where 5.3% increase in IVR efficiency, 55.3% reduction in inductor area and 2X faster performance was achieved; 3) System optimization of a WPT system where 79.1% reduction in receiver coil area and 0.8% improvement in system efficiency were achieved compared to hand-tuned designs along with 67.3% reduction in embedded inductor area for buck converter efficiency >90%. Papers were accepted to COMUS ’17, EPEPS ’17 and a paper was submitted to TVLSI.

**Experimental plan (current year only):** The students have received training to use IBM’s HSSCDR tool where concepts and notations of high-speed channel design and syntax of HSSCDR tool have been presented for generating channels with different interconnect characteristics with emphasis on insertion loss, crosstalk, optimal equalization settings and analysis of eye diagrams. We will investigate applying ML approaches to signal integrity analysis of high-speed channels based on data obtained from the HSSCDR tool. An area we will focus on is identifying worst-case channel interconnect characteristics caused by manufacturing deficiencies. The search space of this problem consists of 19 discrete dimensions, spanning over 5 million different combinations for a given channel topology. The goal is to use ML to find worst-case scenario using minimum number of combinations. We will also investigate the application of uncertainty quantification approaches where we will reduce length of the pulse train for eye diagram and BER analysis by applying kernel estimation method on smaller amounts of data. Rather than rely entirely on randomly sampled data for learning to pick the samples, we propose to incorporate prior learning of knowledge, when available, into learning which include: 1) developing a methodology for generating and selecting pertinent training samples, 2) learning from data based on a “lighted” rather than “black” box, and 3) collecting prior knowledge.

**Related work elsewhere and how this project differs:** ML-based Bayesian optimization methods have been applied extensively in neural engineering. Here, we are modifying these methods appropriately for application to EDA. Prior methods have relied on superposed edge response and statistical eye which tend to have limited use and accuracy.

**Proposed milestones for the current year:** Comparison with non-ML methods; Quantify results based on CPU time and convergence; Software (in Matlab) for implementing TSBO and other Bayesian Optimization based approaches that include strategies for uncorrelated and correlated parameters; Uncertainty quantification and prediction of BER through machine learning; Achieve 10X speedup in eye diagram analysis; Technology transfer to industry.

**Proposed deliverables for the current year:** Software for optimization with 10 or more input parameters; Quantification of the scaling of CPU time with increase in input parameters; Uncertainty analysis and prediction of BER.

**Potential Member Company Benefits:** System optimization solutions involving high dimensional problems (>10); accurate estimation of BER by minimizing simulation runs.

**Estimated Start Date:** 1/1/18  **Estimated Project Completion Date:** Dec. 31, 2018
**Project Summary**

**Title:** Machine learning for trusted platform design  
**Centers:** Center for Advanced Electronics through Machine Learning (CAEML)  
**Tracking No:** 2A2  
**Project Leader(s):** Arijit Raychowdhury (GT) & Madhavan Swaminathan (GT)  
**Phone(s):** (404) 227-0087  
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**Proposed Budget:** $54,345 (year 1)  
**Type:** (New/Continuing/Follow-up) New  
**Other Faculty Collaborator(s):** Chuanyi Ji (GT)

**Project Description:** Several IoT applications are emerging with RF transceivers and Wireless Power Transfer units integrated in a single module. These are smart modules with embedded signal processing. An example of an architectural embodiment is shown in Figure 1 where a single RF carrier is used for bi-directional RF communication and power delivery. Depending on the application, the module may or may not contain an encryption engine (128b AES) for security. Since many of these systems will be autonomous, trusted platforms are required for keeping such objects secure over the product’s lifetime. Such IoT devices are prone to three types of attacks: 1) Side channel attack (SCA) through RF carrier, 2) Power channel attack through power delivery network and 3) EM channel attack through near or far field coupling. Our objective in this project is to use Machine Learning (ML) to i) assess if the system is under attack (ex: identifying constructive and/or destructive links, ii) developing counter measures (ex: shut down the system or modify the security key) and iii) performing i) and ii) in very short time periods (ex: within milli-seconds after the attack occurs).

**Progress to Date (if applicable):** We currently have a prototype of the Wireless Power Transfer (WPT) module functioning at ~1GHz along with models. We also have experience in developing models of RF transceivers and AES (Advanced Encryption Standard) engines. We will use Chip Whisperer board for Power SCA evaluation. We plan to use this prior work to develop data for Machine Learning. In addition, evaluation boards can be used for testing.

**Experimental plan (current year only):** We recognize that model development is hard and model based prediction is computationally difficult due to the high dimensionality of the system. We therefore need to develop models that have high sensitivity to model parameters and have short detection latencies. Our approach therefore is to use Deep Learning techniques that can predict attacks in milli-seconds. We will develop ANN based observers that can be used to monitor internal system states, which allows us to use predictive models and state estimation theory to identify attacks and develop counter measures. As an example, a state estimator (observer) can be trained to detect variations using current and voltage sensors embedded at different points in the power delivery network loop. Changes in the loop’s states can be detected which can be used by the observer to detect attacks.

**Related work elsewhere and how this project differs:** Prior work on security has focused primarily on developing AES engines that are resilient to cyber-attacks. The concept of using an observer is new.

**Proposed milestones for the current year:** Develop ML methods based on both diagnostic and active learning techniques using ANN and Bayesian Inference methods. Apply Deep Learning techniques for detecting minute changes in the system response in milli-seconds.

**Proposed deliverables for the current year:** Models of the system that include RF communication, WPT and security blocks that includes near field coupling through RF coils at ~1GHz using HFSS, ADS and Matlab; Model of observer; Algorithms developed in Matlab for deep learning based on ANN and Bayesian Inference methods; Model based demonstration of identification of cyber-attacks through RF, Power and EM Channels in milli-seconds.

**Projected deliverables for Year 2 (if applicable):** Model based demonstration of counter measures; prototype development with observer; demonstration of trusted platform using prototype or evaluation board; software for deep learning in matlab.

**Potential Member Company Benefits:** Designers must anticipate every form of attack to prevent access to embedded systems and data. Along with already existing work on AES and TPM (Trusted Platform Module), we believe that this approach will provide an added level of security for trusted platform design.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/19
**Title:** Machine Learning to predict successful FPGA compilation strategy  
**Date:** 9/1/2017

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)  
**Tracking No.:** 2A4  
**Project Leader(s):** Sung Kyu Lim (Georgia Tech)  
**Phone(s):** (404) 894-0373  
**E-mail(s):** limsk@ece.gatech.edu  
**Proposed Budget:** $50,000  
**Type:** (New/Continuing/Follow-up) New

**Other Faculty Collaborator(s):** none

**Project Description:** The goal of our project is to build machine learning (ML) models that produce FPGA compilation recipes that show high success rate and fast compilation time. We assume the following are given as the inputs: (1) RTL and its timing constraint, (2) target FPGA device, (3) FPGA compilation toolset (synthesizer, mapper, placer, router), and (4) compilation recipe (optimization goal, effort level, logic restructuring, random number seed, etc.). Our ML model predicts whether the given recipe leads to compilation success (= RTL fits to the FPGA and its timing goals are met). The model also predicts compilation time. For a given set of recipes under consideration, we use this model to select successful ones and order them based on their predicted compilation time. Because ML-based prediction is quick, we can afford to examine many candidate recipes and choose the best one.

The input to our ML model includes circuit structure-related parameters such as the number of LUTs, FFs, global signals, IOs, net-size distribution, etc. Using these inputs, our ML will predict compilation success rate and run time. Our special focus will be on the impact of local congestion on compilation failure. We seek toolset parameters and recipes that effectively avoid local congestion and thus improve success rate and time. We believe that congestion can be considered during all major steps of FPGA compilation. During synthesis, we can choose the options that will minimize the number of nets and pins. During mapping, the connections among different logic elements can be minimized. Placement can be guided to minimize local congestion, while routing is the actual step that decides which routing switches to use and thus a more direct impact on routability. However, congestion avoidance may come at the cost of runtime, timing, and power degradation. Our goal is to seek recipes (and potentially improvement on the compilation engines themselves) that strike a balance between congestion, compilation time, and other key metrics.

We will also build models for silicon interposer-based multi-FPGA systems, where FPGA partitioning becomes a key step in deciding the number of IOs required, demand for interposer interconnects, and ultimately the overall compilation success. FPGA partitioning is performed under a strict pin constraint, which is non-trivial to satisfy. In addition, depending on how partitioning is done, on-interposer routing demand may exceed supply. Our goal is to seek related ML-model parameters and recipes that help alleviate burdens imposed on partitioning.

**Experimental plan (current year only):** We will write codes to access FPGA mapping database, extract key parameters that affect compilation success and runtime, build and train ML models, and process and optimize recipes.

**Related work elsewhere and how this project differs:** Researchers from Tianjin University used ML to optimize FPGA architecture parameters, while Argonne National Lab developed an ML-based tool for FPGA timing and power closure. ML tools from Plunify are producing FPGA compilation recipes for timing closure, and University of Guelph specifically targeted FPGA placement as the key enabler for ML-prediction. However, none of these work address the impact of congestion nor target multi-FPGA systems.

**Proposed milestones for the current year:** Successful recipe constructions and accurate runtime prediction for single and multiple FPGA systems.

**Proposed deliverables for the current year:** Our ML models, scripts, codes, and additional compilation database built in our lab.

**Projected deliverables for Year 2 (if applicable):** Our year 2 plan will target ML models and toolsets that help fix/enhance the original RTL codes to improve compilation success and runtime.

**Potential Member Company Benefits:** Our tool will help Synopsys strengthen their FPGA compilation toolset. In addition, FPGA designers in other member companies will save time searching for good recipes.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/19
Title: Causal Inference for Early Detection of Hardware Failure

Date: 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Tracking No.:** 2A6

**Project Leader(s):** N. Kiyavash, M. Raginsky and E. Rosenbaum (all UIUC)

**Phone(s):** (217) 244-2525; 244-1782; 333-6754

**E-mail(s):** {kiyavash,maxim,elyse}@illinois.edu

**Estimated Start Date:** 1/1/18

**Estimated Project Completion Date:** 12/31/18

**Other Faculty Collaborator(s):**

**Project Description:** A causal inference framework for predicting hardware failures will be developed. The framework will utilize expert knowledge of physics-of-failure and sensor data from the field; sensors monitor performance metrics, environmental conditions, error rate, etc. The methodology will be developed in the context of hard disk drive (HDD) failure prediction since large amounts of sensor and failure data are publically available (from BackBlaze and Baidu storage arrays). HDD “SMART” data include the number of power cycles, number of uncorrected reads, reallocated sector count, temperature, and many other indicators. Our methodology will use the time series data collected through the SMART as well as physical covariates (e.g., temperature) pertaining to a device and to train the predictor. Furthermore, we plan to develop a “causal transfer learning” paradigm that allows us to extend our learning from one device (i.e., one model HDD) to other similar devices. Such a data-driven modeling methodology is ideally suited to capture differences between available device models while avoiding incorrect assumptions about the underlying statistical distributions.

**Progress to Date (if applicable):** N. Kiyavash has developed an information-theoretic framework for causal inference from time series data using both parametric and non-parametric models.

**Experimental plan (current year only):** Evaluate causal inference predictive frameworks using SMART data and HDD failure statistics. Two types of models will be considered for modeling time series SMART data. (1) Non-parametric models for which causal relationships are quantified information theoretically (e.g., using directed information measure). (2) When suitable, parametric models such as autoregressive models or mutually exciting point processes to capture both continuous and discrete events. While parametric models rely on stronger assumptions, they result in reduced sample and computational complexity of the causal inference task. The team will test both types of modeling frameworks to evaluate their suitability for prediction and transfer learning tasks for failure prediction.

**Related work elsewhere and how this project differs:** HDD failure prediction from SMART data has been attempted by several organizations, including UCSD (Murray 2005), Google (Pinheiro 2007), and Nankai-Baidu Joint Lab (Li 2017). Recently, IC field-use data was collected by telemetry and used for knowledge-based qualification of microprocessors (Intel, Kwasnick 2017) and motor drive circuits (Google, Kale 2017). Furthermore, many research groups have worked on benchmarking the life expectancy of their products (or systems) under expected service loads and environmental conditions. Most research in both domains uses simple correlation type metrics or side information about the physics of the system in the form of Bayesian analysis. The longitudinal causal inference techniques advocated here are a major departure from such approaches and allow for principled ways of omitting redundant covariates or features that might be correlated with the failure but do not help in the prediction task.

**Proposed milestones for the current year:** (1) Use domain-specific knowledge to develop statistical models for causal inference. (2) Identify dataset requirements and

**Proposed deliverables for the current year:** (1) Basic demo of a software implementation. (2) Theoretical analysis of algorithm complexity/performance. (3) Technical report to center members.

**Projected deliverables for Year 2 (if applicable):** (1) Large-scale software implementation and validation. (2) Report on cost-benefit analysis and comparison of non-parametric and parametric models.

**Potential Member Company Benefits:** Early detection of component failure may revolutionize system design, e.g. by allowing one to reduce redundancy or lengthen the system lifetime specification. Component failure is of concern on both a micro scale (trillions of Flash memory cells in a solid-state drive) and a large scale (thousands of HDD in a storage array).
<table>
<thead>
<tr>
<th><strong>Project Summary</strong></th>
<th><strong>Title</strong>: Applying Machine Learning to Back End IC Design</th>
<th><strong>Date</strong>: 9/1/17</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Center</strong>:</td>
<td>Center for Advanced Electronics through Machine Learning (CAEML)</td>
<td></td>
</tr>
<tr>
<td><strong>Tracking No.</strong>:</td>
<td>2A7</td>
<td></td>
</tr>
<tr>
<td><strong>Project Leader(s)</strong>:</td>
<td>Davis, Franzon (NCSU)</td>
<td></td>
</tr>
<tr>
<td><strong>Phone(s)</strong>:</td>
<td>(919) 515-7351</td>
<td></td>
</tr>
<tr>
<td><strong>E-mail(s)</strong>:</td>
<td>{wdavis, paulf}@ncsu.edu</td>
<td></td>
</tr>
<tr>
<td><strong>Proposed Budget</strong>:</td>
<td>$53,925</td>
<td></td>
</tr>
<tr>
<td><strong>Type</strong></td>
<td>(New / Continuing / Follow-up) Follow-up</td>
<td></td>
</tr>
<tr>
<td><strong>Other Faculty Collaborator(s)</strong>:</td>
<td>Baron (NCSU)</td>
<td></td>
</tr>
</tbody>
</table>

**Project Description**: In 2017, we proposed a one year project to investigate automating back end flows for ASICs. After being recommend by the IAB, we were asked to break this into three projects (1) back end flows; (2) FPGA flows, and (3) CNN for DRC investigation. In this project, we will two major objectives (1) how to set up a synthesis and physical design flow to meet specific goals, and (2) what the trade-offs are for a design between this setup and the design goals. The first goal towards achieving these objectives will be to determine how to set up the tools for a specific design for specific goals. Both the Cadence and Synopsys backend tools have many options that have a strong impact on the achievable speed, resource allocation and compile time. Surrogate modeling will be used to capture these relationships in a global fashion. The outcome of this step will satisfy both objectives for a specific design. The second goal would be to determine how to achieve this mapping for a variety of designs. Classification techniques will be used to classify designs so that these objectives can be met for a specific design without having to run that design through the tool flow. Instead the design will be run through the classifier and the possible classifications will be used to determine the setup and tradeoffs for that design. Possible classification vectors include net/gate ratio by region, net-span distribution, timing criticality coming out of synthesis, slack distribution, etc. A key objective would be to work out the suitability of various classification vectors. Past work focused on the complete flow including placement and routing. This work will include details on power and clock insertion.

**Progress to Date (if applicable)**: Though not a renewal, a trial investigation found that we could produce a surrogate model with sufficient accuracy for Cadence flows. The production of these models has been automated.

**Experimental plan (current year only)**: We will start by producing surrogate models for a range of designs, both those sourced at NCSU and those obtained by from CAEML member companies. These models will be used to determine that setup automation and tradeoff automation can be easily achieved for a specific design. Then we will start evaluating possible classification vectors that can be used to characterize designs. Vectors will be evaluated for their correlation to design objectives and tool setup alternatives. We will investigate detailed flows for automated power rail and clock insertion.

**Related work elsewhere and how this project differs**: There is no similar work we are aware of.

**Proposed milestones for the current year**: (1) establish the viability of using surrogate modeling to guide tool setup for a specific design and specific design goals, including understanding the impact on tradeoffs; (2) establish the viability of using surrogate models for power rail and clock insertion, and (d) an understanding of how to classify designs so that this goal can be achieved for a class of designs, not just individually characterized ones.

**Proposed deliverables for the current year**: Reports on above.

**Projected deliverables for Year 2 (if applicable)**: Ability to setup the tools to achieve specific objectives for a design, without the need to characterize that design first.

**Potential Member Company Benefits**: Improved design convergence for ASIC back end flows.

**Estimated Start Date**: 1/1/18  
**Estimated Project Completion Date**: 12/31/19
## NEW PROJECT PROPOSALS

### Fall 2018 New Project Proposals

<table>
<thead>
<tr>
<th>Project #</th>
<th>Project Title</th>
<th>Pis</th>
<th>timeline</th>
<th>proposed budget</th>
<th>Thrust</th>
<th>Need</th>
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</thead>
<tbody>
<tr>
<td>P18-1</td>
<td>SL2PPA: Netlist-to-PPA Prediction Using Machine Learning</td>
<td>Lim</td>
<td>2 years</td>
<td>$60k</td>
<td>T2</td>
<td>N1</td>
</tr>
<tr>
<td>P18-2</td>
<td>Fast, Accurate PPA Model-Extraction</td>
<td>Davis (Franzon, Baron)</td>
<td>2 years</td>
<td>$54k</td>
<td>T2</td>
<td>N1</td>
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<tr>
<td>P18-3</td>
<td>Efficient Models for IP Blocks for the Purposes of Evaluating Power Delivery and Thermal Performance</td>
<td>Franzon (Davis, Baron, Lobaton)</td>
<td>2 years</td>
<td>$54k</td>
<td>T2 &amp; T5</td>
<td>N2</td>
</tr>
<tr>
<td>P18-4</td>
<td>RNN Models for Computationally-Efficient Simulation of Circuit Aging Including Stochastic Effects</td>
<td>Rosenbaum (Raginsky)</td>
<td>2 years</td>
<td>$76k</td>
<td>T3 &amp; T5</td>
<td>N2</td>
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<tr>
<td>P18-5</td>
<td>High-dimensional structural inference for non-linear deep Markov or state space time series models</td>
<td>Baron (David, Franzon)</td>
<td>1 year</td>
<td>$54k</td>
<td>T1</td>
<td>N3</td>
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<tr>
<td>P18-7</td>
<td>Causal Inference for Reduced Feature Set Modeling of Electronic System Reliability</td>
<td>Kiyavash (Rosenbaum)</td>
<td>2 years</td>
<td>$70k</td>
<td>T2 &amp; T5</td>
<td>N3</td>
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<td>P18-8</td>
<td>ML for Board Level Analysis</td>
<td>Swaminathan (Rosenbaum)</td>
<td>2 years</td>
<td>$75,328</td>
<td>T2</td>
<td>N4</td>
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<tr>
<td>P18-9</td>
<td>Expedient High-Speed Bus PCB Layout Analysis through Machine Learning</td>
<td>Xu Chen, Schutt-Aine, Cangellaris</td>
<td>2 years</td>
<td>$80k</td>
<td>T2, T3</td>
<td>N4</td>
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<tr>
<td>P18-10</td>
<td>Application of ML for generating Interconnect Models with predictive capability</td>
<td>Swaminathan (Schutt-Aine)</td>
<td>2 years</td>
<td>$75,328</td>
<td>T3 &amp; T4</td>
<td>N4</td>
</tr>
<tr>
<td>P18-11</td>
<td>Pseudo-Supervised Machine Learning for Broadband Macromodeling</td>
<td>Schutt-Aine</td>
<td>1 year</td>
<td>$40k</td>
<td>T2, T3</td>
<td>N5</td>
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<tr>
<td>P18-12</td>
<td>Exploring unknown spaces for Component and System Level Modeling</td>
<td>Vasudevan</td>
<td>1 year</td>
<td>$70</td>
<td>T4</td>
<td>N5 N7</td>
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<tr>
<td>P18-13</td>
<td>Enabling Side-Channel Attacks on Post-Quantum Protocols through Machine Learning</td>
<td>Aydin Aysu (Franzon)</td>
<td>2 years</td>
<td>$54,500</td>
<td>T5</td>
<td>N6</td>
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<tr>
<td>P18-16</td>
<td>Design Space Exploration using DNN</td>
<td>Swaminathan (Franzon, Davis, Rosenbaum, Lim)</td>
<td>2 years</td>
<td>$75,328</td>
<td>T2 &amp; T5</td>
<td>N7</td>
</tr>
</tbody>
</table>
### I/UCRC Executive Summary - Project Synopsis

**Date:** 8/19/18

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Title:** NL2PPA: Netlist-to-PPA Prediction Using Machine Learning

**Tracking No.:** P18-1  
**Project Leader:** Sung Kyu Lim, Georgia Tech  
**Co-investigator(s):**

**Phone(s):** 404-894-0373  
**E-mail(s):** limsk@ece.gatech.edu

**Type:** (New, Continuing\(^1\), or Sequel\(^2\)) New  
**Thrust(s):** T2

**Industry Need and Project’s Potential Benefit to Member Companies:** This proposal addresses the SLA2PPA (system-level architecture to power, performance, area) topic requested by the IAB. Design time and cost saving is the most obvious benefit to all member companies.

**Project Description:** This project aims to build machine learning models and develop associated tools to predict PPA results of a given architecture without having to undergo a lengthy physical design process. We assume that the given RTL is already synthesized so that we focus on predicting the PPA impact of physical design process. Using the predicted PPA results, designers can fix and/or improve RTL in turn. The following figure illustrates the overall flow of our approach.

![Diagram of the NL2PPA approach](image)

The input to our ML model includes the target technology specs (technology node, Vdd, target frequency, etc), netlist info (# IPs/gates/nets, connectivity, etc), physical design options (footprint, placement density, P&R algorithms, clock/power network options, etc), and other key features that will help improve the prediction accuracy. We will implement and compare popular ML approaches to achieve our single-digit accuracy goals. Until the member companies provide us with a design database, we will build our own by conducting physical design with various meaningful design settings.

**Progress to Date (if applicable):** We already own open-source benchmark RTLs, their 2D and 3D IC layouts, and sign-off PPA simulations. We also have access to various commercial EDA tools.

**Work Plan (year 2019 only):** We will focus on feasibility of our approach, whether accurate prediction is even feasible for the SLA2PPA problem.

**Related work elsewhere and how this project differs:** Initial efforts have been made such as predicting routing congestion from placement, etc. Our model does not require partial physical design as the input, but accepts early design options including netlist info and physical design options.

**Proposed deliverables for the current year:** design database, ML model, associated tools

**Projected deliverables for Year 2 (if applicable):** Once our feasibility study proves promising, we will concentrate on improving the models with better feature extraction, better ML models, better database, etc.

**Budget Request and Justification:** $60K (one graduate student and travel support)

**Start Date:** 1/1/19  
**Proposed project completion date:** 12/31/2020
I/UCRC Executive Summary - Project Synopsis

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Title:** Fast, Accurate PPA Model-Extraction

**Tracking No.:** P18-2  
**Project Leader:** Prof. W. Rhett Davis (NCSU)  
**Co-investigator(s):** Profs. Paul Franzon, Dror Baron, and Eric Rotenberg (NCSU)

**Phone(s):** (919) 515-5857  
**E-mail(s):** {wdavis,paulf,dzbaron,ericro}@ncsu.edu

**Date:** 8/31/2018

**Type:** New  
**Thrust(s):** T2

**Industry Need and Project’s Potential Benefit to Member Companies:** Fast and accurate estimation of the impact of System-Level Architecture to Power, performance, and area (SLA2PPA). Specifically, this project focuses on elimination of the complicated gate-level simulations needed to make accurate predictions of power, which typically occur very late in the design process. Extraction of system-level power models is extremely difficult, because the data-points are so few and so noisy, while the number of possible model parameters is so huge. This project will develop a comprehensive data-mining methodology to maximize the accuracy of PPA predictions while minimizing the data-collection effort.

**Project Description:** This work will demonstrate a methodology to extract and validate a PPA model from a parameterized system-level design block. We assume that each block has parameterized RTL source-code and a test-bench with embedded architectural event-counters. The physical-design flow prediction framework developed at NCSU (project 2A7) will manage the generation of physical-design data from RTL and the extraction of performance, area, and static-power prediction models. This project will make use of that flow and add the most important missing piece, which is dynamic power-prediction.

The basic approach for dynamic power prediction will be a machine-learning loop that (1) varies system parameters, (2) generates a gate-level model, (3) simulates to gather switching activity and estimate dynamic power, (4) fits a predictive model according to high-level events, (5) chooses the next set of parameters, and (6) repeats to continue the refinement of the model. The central challenge of this project is to show that these high-level events are meaningful predictors of dynamic power.

To manage the complexity of RTL code, we will reuse the existing AnyCore RISC-V PPA framework developed at NCSU, which generates RTL code for super-scalar processors with 1-4 execution lanes, Issue & Load/Store queue sizes of 16-64, and register-file & reorder buffer sizes of 64-128. These and other architecture parameters will be varied, along with system-environment parameters, such as latency of cache fills and benchmark choices in order to gather switching activity and counts of high-level events, such as branch mis-predicts, register renames, etc. The machine-learning flow will fit the switching activity/dynamic-power model according to these parameters. Time granularities as low as 1,000 cycles will be explored, so that the approach can be shown to work with data-sets with large variance. We will use an open PDK and cell-library so that results can be shared without the need for new license agreements.

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### High-Level Events used as predictors for this model

<table>
<thead>
<tr>
<th>Predictor</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Branch Predictor (BP) lookups &amp; mispredictions</td>
<td>Branch Target Buffer (BTB) accesses &amp; hits</td>
</tr>
<tr>
<td>Instruction Cache accesses &amp; misses</td>
<td>Instruction issues &amp; hits</td>
</tr>
<tr>
<td>Writebacks to Physical Register File</td>
<td>Load &amp; Store hits &amp; misses</td>
</tr>
<tr>
<td>Register Renames</td>
<td>Store-Load forwards</td>
</tr>
<tr>
<td>Commits</td>
<td>Load violations</td>
</tr>
<tr>
<td>Pipeline recoveries</td>
<td></td>
</tr>
</tbody>
</table>

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![Graph](attachment:image.png)
Another challenge of the project will be to determine a model formulation and sampling approach that leads to high predictive accuracy and minimizes the amount of training effort. The plot above shows our progress to date, which is a simple linear model for one architecture variant fit from the 18 high-level events listed and 356 gate-level simulations. The root relative squared error (RRSE) is 0.49, which is much larger than the target RRSE, which is below 0.05. To improve this accuracy, we will explore advanced surrogate-model formulations, including multi-variate probability density functions expressed with a sparse polynomial chaos (PC) expansion, which would allow fast determination of combinations of coefficients to yield the best accuracy. We will also explore adaptive sampling techniques, including a basic genetic/evolutionary algorithm and the more complex LOLA-Voronoi algorithm. If time permits, we will demonstrate this approach in conjunction with a fast, parallel gate-level power calculator developed in partnership with Si2 and IEEE SA P2416 that models temperature variation and a full-range of PVT parameters.

**Progress to Date (if applicable):** We have gathered the dynamic-power data shown in the figure above and fit a simple linear model using the 18 high-level event counters listed. We are currently exploring the implications of this model.

**Work Plan (year 2019 only):** We will begin by gathering data, in an effort to determine the number and ranges of architecture, system-environment, and high-level event parameters to be fit. By the end of six months, we will show our first data-set to illustrate the range of these parameters. The second half of the year will focus on the model-training environment. By the end of the first year, we will demonstrate an initial model-training environment with a simple genetic algorithm.

**Related work elsewhere and how this project differs:** Most PPA research is currently focused on extraction of higher-level power models from predictive models such as McPAT. This effort differs in that it seeks to create high-level models from data gathered either from gate-level simulation or measurement. It makes use of numerical techniques that have been successfully applied to electronic design, but not yet to PPA prediction.

**Proposed deliverables for the current year:** Data-set, training-flow and tutorial on how to train the model, and an analysis of model quality and project outcomes.

**Projected deliverables for Year 2 (if applicable):** An enhanced model-training environment will be demonstrated that includes process, voltage, and temperature (PVT) variation and advanced techniques to handle adaptive sampling larger number of parameters (>100).

**Budget Request and Justification:** $54K/year, including support for 1 student ($30K salary & benefits, $16K tuition), $4K travel, and $4K indirect costs.

**Start Date:** 1/1/19  
**Proposed project completion date:** 12/31/20
### I/UCRC Executive Summary - Project Synopsis

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Title:** Efficient Models for IP Blocks for the Purposes of Evaluating Power Delivery and Thermal Performance

<table>
<thead>
<tr>
<th>Tracking No.</th>
<th>Project Leader</th>
<th>Co-investigator(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P18-3</td>
<td>Paul Franzon (NCSU)</td>
<td>W. Rhett Davis (NCSU), Dror Baron (NCSU), Edgar Lobaton (NCSU)</td>
</tr>
</tbody>
</table>

**Phone(s):** (919) 515-7351  
**E-mail(s):** paulf@ncsu.edu

**Type:** (New, Continuing1, or Sequel2); New  
**Thrust(s):** T2

### Industry Need and Project’s Potential Benefit to Member Companies

Many design tasks require accurate power profile prediction. These include DTCO, floorplanning, power delivery design, etc. This project solves that problem using machine learning and adaption of existing verification environments. This proposal is responding to research need 2, Predictive and Behavioral Modeling for Circuit Reliability Prediction.

### Project Description:

This proposal is addressing the problem of “DTCO for advanced packaging”, especially “design challenges for IR drop, transient inductive noise and enhanced Joule heating effect” (quoting the RFP). For a modern complex digital chip, arriving at a prediction for the composite worst-case heat load/current draw and the composite worst-case di/dt is very difficult, in fact almost impossible. The most common state of the art approach often requires human fitting of the results of functional verification runs for each module. These are then used in an architectural simulator. For example, a past PhD student at NCSU did this as reported in [1]. This process is tedious, time consuming and approximate. In addition, it is likely to miss high current events due to correlated actions across multiple modules.

A less expensive solution would be to use machine-learning techniques to fit a current model and tie that model to an architectural simulator. We plan to do this by re-using the logic verification environment as a source of data, as shown in the Figure on the next page.

The model is produced as follows. In a normal verification environment a System Verilog verification vector generator produces high level vectors that are run on a “Golden model” (“C++ model” in the figure) which is often the architectural model. These high-level vectors are translated by a Register Transfer Language (RTL) vector driver to produce RTL Verilog vectors that are run on the RTL code. Not shown is the use of Scoreboard to compare the results produced by the Golden model and the RTL code.

We add instrumentation to this environment to produce a current model. The RTL code consists of multiple modules. One (or more) of these are included in the netlist (i.e. Gate level) format. Vectors can be extracted from the RTL sim runs to run on these netlisted modules. The netlist is used together with the capacitance files to produce an accurate current model. An ML model-fitting environment is used to fit the model as a function of RTL vector sequences. Netlist modules are rotated in and out throughout the verification runs so that a complete current model for every module is eventually built.

The model is used as follows. The SystemVerilog vector generator is programmed to give a functional vector sequence. This is run on the C++ architectural model. The RTL vector driver runs as before producing RTL vectors for the Current prediction, which uses the current model to predict a current profile that is matched to the state of the architectural model. Furthermore, those functions that produce the worst-case current profiles can be identified and isolated.

The main research component of this proposed methodology is working out how to fit a current model for a module to a sequence of RTL vectors. There are a number of possible approaches that could be employed to produce a current predictor based on an RTL vector input. This is not a linear relationship, since small changes in a binary input can lead to large current spikes (e.g. a ripple carry event). That is why the first thing to try is a neural network; probably a deep fully connected one. One possibility is to create a feed forward network based on an input of a sequence of vectors. Another is to use a recurrent network to capture the temporal relationships that are needed to capture the impact of switching. It might also be valuable to apply a classifier to the input vector sequence. For example, for an adder it might be possible to build a classifier that estimates the amount of switching expected between two successive vectors. This is then used as an input to a linear model.
It is important to show this methodology is accurate. We will compare it with full detailed simulations of shorter sequences to do so. For some designs, we can compare it to measurement.

Once the methodology is established, an interesting possibility will be to generate synthetic benchmarks that can be run on their own to generate worst-case events. This can be done by profiling the results of longer functional simulations and produce shorter sequences that start from known states.

Later in the project, we will tie this current predictor to commercial tools for thermal an electrical analysis.

**Model fitting**

- SystemVerilog Verification vector generator
- RTL vector driver
- RTL code
- Module vector
- netlist
- Model Fitting / Sensitivity Analysis Environment
- Current Model

**Model Use**

- SystemVerilog Functional vector generator
- RTL vector driver
- Current Model
- Current Predictor
- Current Profile

**Progress to Date (if applicable): n/a**

**Work Plan (year 2019 only):** The 2019 work plan will focus first on feasibility demonstration, followed by a demonstration in a verification environment:

- April 2019: Feasibility demonstration of a model for a module based on RTL input vectors.
- December 2019: Demonstration of a fully instrumented flow.

**Related work elsewhere and how this project differs:** Current techniques rely on manually or semi-manual driven model fitting, approximations or running the full design flow down to detailed design. An example of the first technique is from our own past work [1] S. Priyadarshi, W. R. Davis and P. D. Franzon, "Pathfinder3D: A framework for exploring early thermal tradeoffs in 3DIC," *2014 IEEE International Conference on IC Design & Technology*, Austin, TX, 2014, pp. 1-6.

**Proposed deliverables for the current year:** April 2019: Feasibility demonstration.
- December 2019: Verification flow demonstration

**Projected deliverables for Year 2 (if applicable):**

**Budget Request and Justification:** $54K/year, including support for 1 student ($30K salary & benefits, $16K tuition), $4K travel, and $4K indirect costs.

**Start Date:** 1/1/19 **Proposed project completion date:** 12/31/20
I/UCRC Executive Summary - Project Synopsis

Center: Center for Advanced Electronics through Machine Learning (CAEML)

Title: RNN Models for Computationally-Efficient Simulation of Circuit Aging Including Stochastic Effects

Tracking No.: P18-4

Project Leader: Elyse Rosenbaum (Univ. of Illinois at Urbana-Champaign)

Co-investigator(s): Max Raginsky (Univ. of Illinois at Urbana-Champaign)

Phone(s): (217) 333-6754  E-mail(s): elyse@illinois.edu  maxim@illinois.edu

Type: New  Thrust(s): T3 & T5

Industry Need and Project’s Potential Benefit to Member Companies: Design guard banding is employed widely to prevent transistor aging due to HCI and BTI from unduly limiting the long-term yield of an integrated circuit. Performance and cost penalties are incurred from guard banding. The proposed project will facilitate the use of smaller guard bands by allowing aging to be addressed as part of design-technology co-optimization (DTCO). To achieve this, a method for accurate and efficient simulation of circuit aging will be developed. For DTCO, the simulations must cover the range of use conditions, i.e., the “mission profile,” which includes the input vector. Furthermore, the deterministic and stochastic aspects of aging both must be simulated. Physical considerations suggest that transistor degradation will show greater variance as transistor dimensions are scaled down and this claim is well validated by experimental data. Today, aging simulations are too slow to be practical, and the accuracy of yield projections are questionable because tool flows don’t support sampling from non-Gaussian distributions nor do they take into account the correlation between time-zero variance and that arising from aging.

Project Description: Circuit reliability simulators (e.g. Cadence RelXpert) perform transient simulation to obtain the voltage waveform at every terminal of the component transistors. Using either built-in or user-supplied models of HCI and BTI induced degradation, the effective age of each transistor is calculated based on the waveforms and the specified operating time. Finally, a new set of model parameters is generated for each transistor, and the aged circuit is simulated. This procedure is repeated for many different inputs (e.g. input vectors) as well as across process corners, resulting in a long turn-around time. Furthermore, if the circuit being simulated is large, a single SPICE (transistor level) simulation validated by experimental data. Today, aging simulations are too slow to be practical, and the accuracy of yield projections are questionable because tool flows don’t support sampling from non-Gaussian distributions nor do they take into account the correlation between time-zero variance and that arising from aging.

In the previous project 1A6, RNNs were used to construct circuit models for transient simulation. Because the RNN is a behavioral model, it will be straightforward to include operating time as a model input. The RNN output will be a snapshot of the circuit response at a given time. The objective is to learn a single RNN model that can be used to predict the output of the circuit in response to an arbitrary input, both when the circuit is fresh and after it has been operated for a user-specified amount of time. As part of 1A6, the researchers developed a Verilog-A implementation of RNN models so that those models can be used with commercial circuit simulators (e.g., Spectre, HSPICE, and ADS).

The most commonly used formulation of the RNN is in discrete time. In project 1A6, we convert the trained RNN from discrete time to continuous time, for compatibility with commercial (SPICE type) circuit simulators, which use a variable time step. As a result of the discrete to continuous time transformation, the final set of equations includes a term $\alpha \cdot h$, where $h$ is the time-step of the training data and $0 < \alpha < 1$; the numerical stability of the model is affected by the choice of $\alpha$. Here, it is proposed to use continuous-time RNNs. This will eliminate the need to both identify a suitable value of $\alpha$ and to provide training data with a constant time step. It is important to ensure that a stable model is learned during the training process. In 1A6, a regularization term (penalty term) was added to the cost function and that remains our favored approach. The identification of a suitable stability criterion will be aided by ongoing work in project 1A1, which seeks to extend previous works on stability analysis of continuous time RNNs in order to formulate stability criteria that are not overly restrictive for circuit modeling.

A circuit’s input-output relationship has a stochastic component due to manufacturing variations (“process variations”) as well as to the non-deterministic trap creation and charge trapping processes that underlie transistor aging. This project will develop a method to encode the stochastic aspects of the input-output relationship in the RNN model. Bayer demonstrated a stochastic recurrent network by adding latent variables to the recurrence equation; another potential approach is to treat the elements of the weight matrices as random variables rather than fixed deterministic constants. It is well known that transistor parameter shifts (e.g. $\Delta V_{TH}$) due to BTI do not follow a Gaussian distribution, and thus we will need to consider alternative probabilistic models for the RNN parameters that will provide a good description of the population of aged circuits.

If a parameter’s mean degradation is independent of its time-zero variability, then the variances will be additive and the generative models for time-zero variability and aging variability can be sampled independently. Degradation due to BTI
is widely assumed to be independent of time-zero variability, i.e., parameter drift is independent of the parameter initial value. However, there are data that suggest a weak correlation. In contrast, there is clear evidence that degradation due to HCI is correlated with the initial parameter values for a given sample; in fact, the distribution of parameters such as $V_{TH}$ may be narrowed by aging. We will initially assume that the two processes are independent (the error introduced will result in conservative projections of reliability) and later develop a procedure to handle the correlation.

The input and output of the RNN may not be what the circuit designer considers to be the input and output signals. To illustrate, consider the simple case of a circuit that implements the Boolean function $Z = A + B$ (NOR gate). A completely general RNN model would take $V_A$, $V_B$, $V_{DD}$ and $V_Z$ as its inputs and $I_A$, $I_B$, $I_{DD}$ and $I_Z$ as its outputs. The general model can handle all of the following: (i) variable load at node $Z$; (ii) slew rate at nodes A and B that varies with the strength of the driver; (iii) supply voltage droop or simultaneous switching noise. This project will develop procedures to generate adequate training data even for the case of a completely general RNN model. A full factorial design of experiment is not feasible, because the training data are obtained from time-consuming transistor-level SPICE simulations of fresh and aged circuits. Referring back to the NOR gate, the voltage waveform at node $Z$ (which is an input to the RNN) is not independent of the voltage waveforms at nodes A and B; however, the dependency is affected by the load at $Z$.

During RNN training, one may encounter the vanishing gradient problem, which prevents the learning of an accurate model for transient simulation. The problem arises if the ratio $\tau/h$ is too large, where $\tau$ is the characteristic response time of the system being modeled. We observe the vanishing gradient problem to occur during circuit modeling only if the system being modeled contains the die as well as off-chip passive elements; therefore, it is not expected to pose a significant problem for modeling of IP blocks or library cells, with the notable exception of edge-triggered registers. This claim is made even though aging proceeds on a much slower time scale than the transistor switching delay because operating time will be a scalar input to the model, similar to, say, temperature. In the event that the vanishing gradient problem arises, Raginsky has suggested adding one new (scalar) term to the recurrence equation that should enhance the model’s ability to capture long-term dependencies; for additional flexibility, we can add a tunable coefficient for every state-space dimension, thus allowing for learning of multiple (and possibly widely separated) time constants.

The RNN model of each library cell will be validated during the training process. When the various RNNs are connected together to emulate a larger circuit, the simulated overall response must be correct. If the per-cell model errors are additive, the simulated response of the full circuit could be highly inaccurate. Project 1A1 is using techniques from nonlinear system analysis to identify conditions under which various interconnections of learned RNN models will provide a stable and accurate approximation to an unknown composite system. We will build on this toolbox to address the above problem of accurately predicting the overall system response.

Progress to Date: In project 1A6, a novel regularization term was introduced to ensure that the learned (discrete time) RNN is Lyapunov stable. A Verilog A implementation of the RNN was developed.

Work Plan (year 2019 only): Train continuous time RNN (CTRNN) to emulate a circuit. Enforce stability of the CTRNN circuit model. Introduce stochastic parameters into RNN circuit model.

Related work elsewhere and how this project differs: The proposed work uniquely seeks to address two challenges simultaneously: (1) eliminate the need to run transistor-level simulation for every input waveform of interest; (2) model the stochastic component of aging. To our knowledge, only Maricau and Gielen have addressed both challenges; they construct a response surface model to map from a transistor parameter distribution to a circuit performance distribution. However, in that prior work, very simple statistical distributions for just a small number of transistor parameters are assumed a priori. 10. E. Maricau & G. Gielen, IEEE Trans. CAD, Dec. 2010.

Proposed deliverables for the current year: How-to guide for training a CTRNN using data obtained by circuit simulation. Manuscript on CTRNN circuit models.

Projected deliverables for Year 2: Report or manuscript on modeling the distribution of aged circuits, accounting for dependency on time-zero variability. Procedures for ensuring end-to-end accuracy of concatenated RNN models.

Budget Request and Justification: $76,000. 1.5 graduate research assistants; one student will be half-time on 1A1. Travel to the CAEML meetings and 1 conference. Computing charges.

Start Date: 1/1/19 Proposed project completion date: 12/31/2020

### I/UCRC Executive Summary - Project Synopsis

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Title:** High-dimensional structural inference for non-linear deep Markov or state space time series models

<table>
<thead>
<tr>
<th>Tracking No.</th>
<th>Project Leader</th>
<th>Co-investigator(s)</th>
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<tbody>
<tr>
<td>P18-5</td>
<td>Dror Baron (NCSU)</td>
<td>W. Rhett Davis (NCSU), Paul Franzon (NCSU)</td>
</tr>
</tbody>
</table>

**Phone(s):** (919) 513-7974  
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**Type:** New  
**Thrust(s):** T1

### Industry Need and Project’s Potential Benefit to Member Companies:
In many applications, a time series of high-dimensional latent vector variables is observed indirectly from noisy measurements. As a motivating application, consider an array of hard drives that are prone to possible failure, where data about the drives’ performance is collected. The data is later used to predict possible future failures, and the system can respond accordingly. A common challenge in these systems is that the data is very high-dimensional, and conventional machine learning approaches suffer from the so-called curse of dimensionality.

### Project Description:
One approach to reduce the dimensionality of time series data uses conditional mutual independence (CMI) to prune variables that seem redundant. That said, CMI-based processing may still result in hundreds or even thousands of variables. While approaches such as recursive neural networks (RNN) have been very successful with low-to-moderate dimensionality levels, it is unclear whether they scale in a computationally tractable manner.

Our goal is to evaluate whether other approaches might scale better in high-dimensional settings. One possible approach by Krishnan et al. uses deep Markov models (DMMs), where an inference network approximates a posterior probability for the time-dynamics of latent variables by running a multi-layer perceptron (MLP) neural network. Moreover, the Markovian property of the DMM data helps simplify the analysis, leading to a computationally tractable approach to optimize a Kullback-Leibler divergence term. We will implement and develop a DMM system that can cope with various types of statistical structure among the features, and pay close attention to scaling the computation as the dimensionality increases.

### Progress to Date (if applicable):
We are currently performing a literature review on DMM, and plan to carry out preliminary testing using the algorithm by Krishnan et al.

### Work Plan (year 2019 only):
After implementing Krishnan et al.’s DMM approach, we will optimize and benchmark its performance against other applicable methods, allowing us to transition to higher-dimensional data. Extra steps we envision include: (1) testing the data for the Markov property and (2) exploring data structures that are amenable to fast computation, possibly including GPU implementation.

### Related work elsewhere and how this project differs:
While the ongoing project 2A6 has used conditional mutual independence (CMI) to prune variables that seem redundant, it has not considered how to process data sets that are still high-dimensional after the pre-processing pruning step.

### Proposed deliverables for the current year:
1. Develop an algorithm designed for high dimensional sequential data analysis;
2. Integrate the algorithm with the CMI-based approach; and
3. Publish the results and evaluate real-world applications.

### Projected deliverables for Year 2 (if applicable):
To be determined based on our progress. Ideally, we want to integrate our approach to CMI-based approaches and other ongoing CAEML projects.

### Budget Request and Justification:
$54K/year, including support for 1 student ($30K salary & benefits, $16K tuition), $4K travel, and $4K indirect costs.

**Start Date:** 1/1/2019  
**Proposed project completion date:** 12/31/2019
I/UCRC Executive Summary - Project Synopsis

Center: Center for Advanced Electronics through Machine Learning (CAEML)

Title: Causal Inference and Dimension Reduction for Modeling of Electronic System Reliability

Tracking No.: P18-7

Project Leader: Negar Kiyavash (Georgia Tech.)

Co-investigator(s): Elyse Rosenbaum (University of Illinois)

Phone(s): (217) 721-5307 (NK); (217) 333-6754 (ER)

Type: Sequel

Thrust(s): T2 & T5

Date: 08/30/2018

Industry Need and Project’s Potential Benefit to Member Companies: The electronics industry generates a large amount of data, primarily to detect if a process goes out of control, but it does not fully exploit the data. As one example, both HDD and SSD can report S.M.A.R.T. attributes to a central server, allowing the data center owner to determine if temperature remains within specified limits or if the number of uncorrectable errors for one make of drive is high. As another example, semiconductor foundries perform electrical measurements on transistor, resistor, and interconnect test structures of many different geometries. If any of the extracted parameters suddenly go outside specified limits, the fabrication line may be shut down until the underlying problem is identified and solved. The proposed project seeks to utilize those data to predict events that will occur at a later time. Causal inference is a method for selecting the most relevant features; having a too large number of features can reduce the performance of the learners and classifiers. Features are inputs to a model; the most useful models will provide probabilistic answers to counterfactual question, e.g., "How long would drive X last if it were subjected to a workload pattern Y from this point forward?" Building on project 2A6, the proposed work will benefit the member companies by allowing them to identify components that will soon fail or designs that have a high likelihood of low long-term yield, while the new thrust on structured inference will enable the members to adjust workloads to maximize component lifetime.

Project Description The proposed project has two thrusts: causal structure learning and structured inference modeling. In the current CAEML project 2A6, we initiated investigating the use of causal inference with conditional mutual independence for selecting the most relevant features. The selected application was cloud storage systems reliability. HDDs and SSDs can be monitored periodically for many different features, such as read error rate, internal temperature, etc., by means of the built-in S.M.A.R.T. – self-monitoring analysis and reporting technology. Favorable results were obtained (see section “Progress to Date”); however, the number of SMART attributes that get recorded rarely exceeds 20 and thus this is not an ideal application in which to evaluate the scalability of causal structure learning. Here, it is proposed that the techniques developed in 2A6 be applied to applications in which the size of the feature set is larger by at least an order of magnitude. In parallel, we will develop structural inference models for failure prediction; such models will account for future use conditions.

Feature selection for high-dimensional datasets: Causal inference remains the focus of this project; however, in high dimensions (number of features in hundreds or even thousands with inadequate sample size), conditional independence-based causal structure learning via conditional mutual information estimation does not lead to acceptable performance. We will develop approaches suitable for large datasets generated by CAEML member companies. Two promising techniques have been identified: (i) Dimensionality reduction by feature clustering; (ii) More efficient learning of the directed graph by means of linear modeling. In the first technique, the first step is to cluster the features based on a notation of similarity or correlation among them. Next, the structure learning is performed only on the representatives of each cluster. In the second technique, if the structural model generating the data can be estimated as a linear model or an additive noise model, one can utilize regression-based methods (e.g., LiNGAM\(^1\)) for structure learning. These approaches perform better in high dimensions compared to conditional independence-based methods.

One application for the feature selection algorithms is to identify those circuit designs that will have low long-term yield in a given process technology. A small subset of IC designs suffer reliability problems in the field. We seek to determine whether the time-zero measurement data combined with key design attributes can be used to identify which IC designs will have compromised reliability in the particular process technology (industry contact: T. Nigam, GlobalFoundries). Local layout effect (LLE) modeling (GlobalFoundries) is another prospective application. Additional applications will be explored in collaboration with the CAEML industry members, e.g., data-driven SSD reliability models that take advantage of diagnostic, internally logged firmware signals.

Structured inference: The lifetime of a solid-state device, including but not limited to SSD, is highly dependent on its past and future workload\(^2\). This observation motivates the development of a generative state-space model to predict SSD lifetime and answer counterfactual questions in the realm of failure prediction. Such a model would allow datacenter management to predict storage drive lifetime given future workload conditions and potentially design tailored workload.
patterns to extend drive lifetimes. We propose to utilize the work of Krishnan et al. on deep Markov models (“DMM”) for structured inference\textsuperscript{3}. SSD failure prediction in cloud storage systems will be the initial application for this work. SSD SMART and failure data have been obtained from researchers at Google; some of the SSD SMART attributes contain information about workload. Markov-type time series models provide a framework for learning dynamic representations of drive health from usage inputs (e.g., data read/write rates), diagnostic information (e.g., bad and reallocated sector counts), and the drive history. DMM are particularly appealing for this application because they are robust even in the face of missing data entries, which is a significant issue for all of the SMART data sets we’ve examined.

In the latter part of this project, we will evaluate the feasibility of extending the work on structured inference to larger problems, such as the modeling of computer system performance (contact: C. Cheng of HPE).


**Progress to Date:** In 2A6, casual structure learning was used to discover conceptually necessary features for the task of prediction. Our approach is motivated by the concept of Granger causality and structure learning for Bayesian networks. The main tool used in this method is performing conditional independence tests for finding direct causes of the target variable, the failure of the disk drive. In 2A6, we identified a conditional independence estimator that is applicable to datasets containing mixed random variables: discrete and continuous. Majority of the prior work focuses on applying standard supervised machine learning approaches to the SMART attributes in order to obtain predictors for failure time. The state-of-the-art performance in this area was achieved by Xu et al.\textsuperscript{2}; those authors reported a detection rate of 97.71\% with a false alarm rate of 0.06\% on their data. Inspired by that favorable result, we train a GRU-type recurrent neural network on the selected features. We evaluated this approach on a small dataset with 12 features. We detected 7 features as direct causes of the target variable. Our primary results show that we were able to obtain almost exactly same performance compared to the case of using all 12 features:

- RNN (all 12/12 features): Detection Rate: 98.85\%, False Alarm Rate: 0.109\%.
- RNN (selected 7/12 features): Detection Rate: 97.70\%, False Alarm Rate 0.109\%


**Work Plan (year 2019 only):** In thrust one, structure learning, we will work with GlobalFoundries and other members to develop tools for deriving insights from their high-dimensional manufacturing data. We will investigate the clustering method and the performance under linear model approaches on this data. In the second thrust, structured inference, we plan to build upon our progress-to-date by developing new models and techniques for the SMART-type data investigated in project 2A6. We will start with the DMM as a guideline for our generative model but will modify the design as needed to meet the needs of the SSD data. We will use this model for the task of robust failure prediction in the case of missing entries in the Google dataset. We will use our GRU-type recurrent neural network from project 2A6 as a baseline for evaluating the quality of our structured inference model. We will further use this model to develop a counterfactual based policy learner which is capable of estimating the optimal policy based on the generated data to design the optimal workload pattern for any state of the system.

**Related work elsewhere and how this project differs:** HDD failure prediction from SMART data has been attempted by several organizations, including UCSD (Murray 2005), Google (Pinheiro 2007), and Nankai-Baidu Joint Lab (Li 2017). Most research groups have worked on benchmarking the life expectancy of their products under expected service loads and environmental conditions. Yet they use simple corellelative metrics or side information about the physics of the system in the form of Bayesian analysis. The longitudinal causal inference techniques advocated here are a major departure from such approaches and allow for principled ways of omitting redundant covariates features. Recent work on utilizing neural architectures to form structured inference models such as (Kingma et al. 2013), (Rezende et al. 2014), and (Mine et al. 2014) use ideas from deep neural networks to derive generative models. (Krishnan et al. 2017) proposed a deep Markov model, a class of generative models in which linear emission and transition distributions in classic hidden Markov model are replaced with complex multi-layer perceptrons. Prior works on structured inference do not consider applications in the realm of electronics reliability or design.

**Proposed deliverables for the current year:** First thrust: Reporting the results of testing linear models on data. Second thrust: Reporting feasible generative models and testing these models on our available dataset.

**Projected deliverables for Year 2 (if applicable):** Extension of our results to larger datasets and across industries and producing a software tool that could be used by the partners.

**Budget Request and Justification:** Projected annual cost of approximately $70,000 to support two graduate students (one on a fellowship), 0.5 month summer salary for lead PI, and travel costs.

**Start Date:** 1/1/19  \hspace{1cm} **Proposed project completion date:** 12/31/20
**I/UCRC Executive Summary - Project Synopsis**

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Title:** ML for Board Level Analysis

**Tracking No.:** P18-8

**Project Leader:** Prof. Madhavan Swaminathan

**Co-investigator(s):** Collaborators include Prof. Elyse Rosenbaum (UIUC)

**Phone(s):** (404) 894-3340

**E-mail(s):** madhavan.swaminathan@ece.gatech.edu

**Date:** 08/17/2018

**Type:** New

**Thrust(s):** T2

**Industry Need and Project’s Potential Benefit to Member Companies:** The ML ecosystem to be developed in this project will provide a fast & accurate way for a thorough analysis of complex high-speed PCB, package or interposer designs. In addition, individual blocks in the proposed ecosystem can be very beneficial for tasks other than worst-case net detection, such as design space exploration and optimization either at the topological, geometrical or circuit level of high-speed channels. Research Need: Worst-case SI net identification in high-speed bus PCB layout designs.

**Project Description: The Problem:** The emerging demand in high performance computing has led to the need for high bandwidth chip-to-chip communication channels. As the data rates increase, these high-speed channels are required to be simulated by full-wave EM solvers over a large frequency bandwidth to accurately characterize the crosstalk between different signal paths and reflections caused by discontinuities, which are collectively represented by multiport S-Parameters. Typically, a high-speed PCB contains hundreds to thousands of such channels, which makes the use of full-wave EM solvers infeasible in practice as such a large-scale simulation at the board level have unacceptable CPU time and memory requirements. Hence, designers tend to investigate the board file to determine a “worst-case net”, the channel that is likely to contain the highest amount of reflections and crosstalk, and analyze it to ensure that the final system supports the required data rates. This worst case representation of the system may result in over-designing the system as other nets in the PCB can have relatively better electrical performance compared to the worst-case net and the overall system performance can be increased substantially by improving the design rules of only a few nets.

**Proposed Solution:** In this project, we plan to build a machine-learning (ML) based ecosystem to perform board level analysis of a given PCB, characterize the electrical performance of each net and rank them in descending order of eye openings to identify the worst-case scenario, as well as the relative performance of every other net in the PCB with respect to the identified worst-case net. We anticipate the ML ecosystem to contain 3 main blocks, namely a translator, frequency and time domain predictors.

As the input to the ecosystem is intended directly to be a board file, it needs to be converted into structure that can be interpreted by mathematical models. For this, we anticipate use of image detection/classification techniques based on region of interest (RoI) algorithms that are widely used in ML community, such as graph-based saliency detection [1], to identify structures in each signal path, including signal-to-ground ratio in via array, length of pin-area wiring, spacing between victim and aggressors etc. The output of this stage will be structures and their corresponding parameters of each net in the PCB.

The identified structures in each net will then be used by the frequency domain predictor. This block is anticipated to contain a library of parameterized predictive models of transmission lines and via arrays to generate S-Parameters of each component in the signal path and cascade them according to the structure provided by the translator block. Along with geometrical parameters, we will be including topological parameters to the model library, such as stack-up structure, signal-to-ground ratio, number of aggressors etc. We will build upon our work on Bayesian Active Learning using dropout (BAL-DO) [2] and Two-Stage Bayesian Optimization (TSBO) [3] by developing multi-fidelity and transfer learning techniques to handle complexity of creating a rich library that require very CPU extensive simulations to characterize. The dropout and hierarchical partitioning tree developed for BAL-DO and TSBO will be adapted & extended to include topological parameters and reduce CPU time required for deriving these accurate predictive models. The output of this block will be the end-to-end S-Parameters of each net. Since the number of nets will be in the order of thousands, we will investigate using variational inference techniques to speed-up prediction times rather than exact inference required to perform a fully Bayesian analysis.
Once the S-Parameters of each net have been generated, frequency domain features that represent this large S-Matrix will be extracted, combined with TX/RX driver settings including equalization parameters and then used by Time Domain Predictor model to predict eye height & width at a certain BER contour. By deriving a predictive model where the inputs are frequency domain features rather than geometrical & topological parameters, we plan to “abstract” the physical structure of the channel to make the model more generic. We will build upon frequency domain features that IBM currently uses to estimate if a channel satisfies the eye opening margins without actually doing the time domain simulation [4]. The output of this block will be the predicted eye width, height and jitter of every signal path in the PCB file, which will be ranked to determine the worst-case net. As we anticipate the level of non-linearity of the model derived for Time Domain Predictor is to be substantially higher compared to other blocks, we will investigate the use of Deep Gaussian Process models.


Progress to Date (if applicable): We have developed a fast & accurate Bayesian Active Learning algorithm [2] and an effective hierarchical sampling strategy [3] as part of CAEML to be used for efficient generation of library of models in Frequency Domain Predictor. We will also leverage the work done by IBM [4] for abstracting the physical channel structure to operate directly on frequency domain features of a channel.

Work Plan (year 2019 only): We will start building the ML ecosystem by Time Domain Predictor block for a fixed TX/RX driver topology but with parameterized equalization settings. Then, we will define features for abstracting TX/RX drivers, similar to features derived in [4], and include these in our model for a generic predictor that takes circuit topology and S-Parameters of the channel as input to predict eye characteristics.

Related work elsewhere and how this project differs: Board level analysis can’t be done with 3D EM accuracy. Commercial “parasitic extractors” use various approximations, which is not acceptable for high-speed channels. The proposed board-level analysis ecosystem is new and expected to be fast & have substantially higher accuracy, accompanied with confidence intervals around predictions to be used to assess the model/prediction quality.

Proposed deliverables for the current year: 1) A MATLAB code for Time Domain Predictor that can predict eye width, height and jitter directly from S-Parameters and TX/RX settings, without time domain simulations. 2) Preliminary version of the Frequency Domain Predictor for proof of concept.

Projected deliverables for Year 2 (if applicable): 1) A MATLAB code for Frequency Domain Predictor for a rich library to handle geometrical & topological control parameters. 2) A MATLAB/Python code for translator block and demonstration of board-level analysis.

Budget Request and Justification: Year 1: $75328 (1 full time GRA for 12 months; 25% Post Doc; $5K travel); Year 2: $77416 (1 full time GRA for 12 months; 25% Post Doc; $5K travel).

Start Date: 1/1/19 Proposed project completion date: 12/31/2020
I/UCRC Executive Summary - Project Synopsis

Date: 08/30/2018

Center: Center for Advanced Electronics through Machine Learning (CAEML)

Title: Expedient High-Speed Bus PCB Layout Analysis through Machine Learning

Tracking No.: P18-9
Project Leader: Xu Chen (University of Illinois at Urbana-Champaign (UIUC))
Co-investigator(s): Andreas Cangellaris, Jose Schutt-Aine (UIUC)

Phone(s): (217) 244-7279   E-mail(s): xuchen1@illinois.edu, cangella@illinois.edu, jesa@illinois.edu

Type: (New, Continuing, or Sequel) New  Thrust(s): T2, T3

Industry Need and Project's Potential Benefit to Member Companies: There is a pressing industry need for machine-learning methods for post-route PCB physical layout inspection and fast identification of those nets that will exhibit the worst-case bit-error rate. CAEML member companies have identified this need as one of high-priority for them in their quest for reduced design completion time, reliable avoidance of over-engineered designs and reduction of design cost.

Project Description: Present-day high-speed digital systems require the transmission of data at multi-gigabit rates over links where signal degradation due to losses, crosstalk, and discontinuities is prominent. Intersymbol interference limits the maximum data rate and is analyzed and demonstrated using eye diagrams at various bit rates. In modern systems, error rates are usually very low. Therefore, to analyze reliably the impact of layout and geometrical parameter variations on bit error rate (BER), very long simulations sequences are needed. Behavioral high-speed link simulators, such as IBM’s HSSCDR, enable evaluation of BER faster than transient simulators, but accurate S-parameter models of the channel must be generated using time-consuming full-wave electromagnetic solvers. For large designs with many nets, it is desirable to limit the modeling effort on the worst-performing nets. This project will apply state-of-the-art machine learning (ML) techniques to develop the capability to automatically identify the worst-case nets via computer-aided inspection of the layout, providing also anticipated BER performance. In this manner, significant gains can be realized in the tedious and time-consuming post-route analysis.

Artificial neural networks (ANN) are good contenders for machine learned solutions and will be used for the purposes of this project. Our approach will take advantage of our extensive experience and suite of tools developed by our group for fast, stochastic electromagnetic (EM) modeling and circuit simulation of high-speed interconnects, which exhibit uncertainty in their geometric, material and layout parameters and, thus, require that the output or response parameters as characterized in the probability domain. In particular, we have developed a suite of non-intrusive, stochastic collocation (SC) methods, which converge faster than Monte Carlo methods, and are fully compatible with existing verification workflow including commercial EM/circuit solvers and proprietary high-speed link simulators such as HSSCDR. Using the cost function defined as the BER of the link, with random inputs identified, including variability in trace cross-sectional geometry, aggressor spacing, via geometry and layout, and accounting for the various types of discontinuities and reference-plane imperfections encountered in PCB interconnects, our SC suite will be combined with full-wave solvers and fast extractors to provide for the expedient calculation of the responses of the extensive set of different instantiations of links needed to train the neural network. The training of the neural network will be expedited using the variational auto-encoder (VAE) generative techniques we have developed and demonstrated under CAEML Project 1A1. Using SC, the sensitivity of BER with respect to the unknown parameter(s) can be quantified, in order to expedite the identification of worst-case net. The PIs have previously demonstrated that SC is effective for predicting eye-width of nets with random parameters [1]. The PIs have also demonstrated that SC can be used to perform optimization in random space [2]. Hence, we are confident that SC can be used in the context of the proposed project to identify worst-case nets based on metrics such as eye-width and BER.


Progress to Date (if applicable): N/A

Work Plan (year 2019 only): Our effort during Year 1 will focus on the following three tasks: A) Quantification of the sensitivity of channel BER to the various layout/geometric/material interconnect and discontinuity parameters and their uncertainty. B) Development of the computational framework for the use of SC and a VAE-accelerated algorithm in
conjunction with fast extractors and IBM’s HSSCDR for the fast calculation of the BER of a sufficiently extensive set of
different instantiations of nets for the training of the neural network. C) Proof of concept of the predictive capability of
the proposed machine-learning approach to worst-case net identification.

**Related work elsewhere and how this project differs:** To our knowledge, no machine learning-based tool or
effort is available for post-route PCB layout evaluation.

**Proposed deliverables for the current year:**
A) Tool for translating PCB layout to format compatible with ANN. B) Implementation of SC capability in HSSCDR; C) Train neural network to predict eye-width and BER based on S-parameters.

**Projected deliverables for Year 2 (if applicable):**
A) Train neural network to predict eye-width and BER based on layout and geometry parameters
B) Computational framework for fast training of a Neural Network for ML-based identification of worst-case nets.

**Budget Request and Justification:** We request a budget of $53,350/year. An itemized budget is attached. This will include support for a graduate student, as well as partial faculty support for the PI. We also request some budget for purchasing equipment and travel to CAEMI workshops and conferences to present our results.

| Start Date: 1/1/19 | Proposed project completion date: 12/31/2020 |
### I/UCRC Executive Summary - Project Synopsis

**Date:** 08/17/2018

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<td><strong>Title:</strong></td>
<td>Application of ML for generating Interconnect Models with predictive capability</td>
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<td><strong>Tracking No.:</strong> P18-10</td>
<td><strong>Project Leader:</strong> Prof. Madhavan Swaminathan</td>
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<tr>
<td><strong>Co-investigator(s):</strong> Collaborators include Prof. Jose Schutt Aine (UIUC)</td>
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<td><strong>Type:</strong> (New, Continuing?, or Sequel?) New</td>
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<td><strong>Thrust(s):</strong> T3/T4</td>
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#### Industry Need and Project’s Potential Benefit to Member Companies:
Long and complex interconnects have two fundamental problems for model development: 1) Rational function models require numerous poles making the model complex and 2) any reduction in poles causes causality related issues. We plan to address both of these problems through this project. Research Need: Efficient high-speed interconnect modeling through machine learning.

#### Project Description: The Problem:
The standard method of modelling delay for coupled interconnect systems is by using low order rational functions. The low order polynomials gives the general problem of fitting for wide frequency range of frequency [1]. This fitting problem is often solved by using the popular method of vector fitting which is based on doing the approximation in two stages, both with known poles as: (i) the poles are distributed over the frequency range of interest and (ii) fitting of an unscaled function from the new set of poles computed from stage 1 [2]. But modern day coupled interconnect systems are laden with discontinuities and non-constant delays due to dispersion or multiple delays from the various modes. Additional delays come from the DDR memory paths that contain tees and multi-drop interconnects. The method of vector fitting does not work well in reduction of model complexity. The machine learning method for efficient reduced order modeling (ROM) of coupled interconnect systems using pole clustering improves over the rational function fit, but the problem of causality and passivity remains.

#### Proposed Solution:
In this project as shown in Figure 1, we plan to develop a Generative Adversarial Neural Network (GAN) Model for computing the delay of complex interconnect systems, while satisfying the causality and passivity constraints [4]. The discriminator neural network (DNN) part of GAN is trained on the input set of pole distribution where it classifies input poles using discrete classes such as class 0, class 1 etc. The DNN is trained to classify poles from various input pole distributions using statistical features of pole distributions. Each class is associated with its own causality and delay measures and this knowledge comes from literature and domain engineering that is stored in a separate memory database as shown in Fig 1. Then the trained classifier DNN is played against a Generative Neural Network (GNN), which produces a completely new class of poles. The protocol of the adversarial game we propose for this project to be played between DNN and GNN is as follows:

1. **GNN generates a completely new class of poles using the Wasserstein distance**
2. **DNN verifies whether it has seen it before this class in its training set**
3. **DNN shares the result with GNN at the end of verification in this handshake protocol. Each of DNN and GNN are rewarded/punished accordingly.**
4. **DNN estimates the causality measure if the class generated by GNN is completely new else DNN discards the class if the class generated by GNN is a known class.**

In the proposed approach, the GNN generates all possible new classes of poles (along with the constraints of causality and passivity) by moving in its latent space. The GNN creates new constrained class of poles, by creating a completely new distribution using the metric of Wasserstein distance. This new constrained class of poles are verified by DNN and its corresponding estimated delay is stored in the memory database for future training. Our method of computing delay parameter (and also verifying causality and passivity) using GANs method improves over the method of pole clustering as it can compute its own delay parameters for any new complex circuits every time. The new complex circuits will have its own distribution of poles and our GAN will create a new class of poles, while satisfying any constraints of causality and passivity every time. The training is done in linear time and classification of new class of poles is done in constant time.
Progress to Date (if applicable): We have built our classifier DNN on the Tensorflow framework and trained faster each batch of poles in parallel by an Amazon EC2 instance. Each of these Amazon EC2 instances are created on the fly for training and is deleted on completion.

Work Plan (year 2019 only): The work plan consists in developing a scalable machine model for accurate extraction of delay content from complex interconnect systems while satisfying causality and passivity constraints. This requires building a scalable Generative Adversarial Network (GAN) in Tensorflow framework in distributed cloud for computing the delay. Then we will built a multi-environment software interface that translates the outputs (frequency response) from complex circuit models to our Generative Adversarial Network (GAN) model.

Related work elsewhere and how this project differs: Prior work is available from [3] in the area of applying rational functions and pole clustering. Based on discussions with the author, our proposal addresses issues related to delay and causality.

Proposed deliverables for the current year: 01/19-06/19: Development and implementation of GANs. 07/19-12/19: Application and validation for generating new class of poles using GANs, and computing delay for new complex interconnect systems, while satisfying causality constraints.

Projected deliverables for Year 2 (if applicable): Development of mapper and application to complex systems. Fine tuning of the method.

Budget Request and Justification: Year 1: $75328 (1 full time GRA for 12 months; 25% Post Doc; $5K travel); Year 2: $77416 (1 full time GRA for 12 months; 25% Post Doc; $5K travel)

Start Date: 1/1/19  Proposed project completion date: 12/31/2020

Figure 1: Generative Adversarial Networks pipeline for new class of poles generation for computing delay
I/UCRC Executive Summary - Project Synopsis

Center: Center for Advanced Electronics through Machine Learning (CAEML)

Title: Pseudo-Supervised Machine Learning for Broadband Macromodeling and Circuit Synthesis

Tracking No.: P18-11

Project Leader: Jose Schutt-Aine, Maxim Raginsky

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Type: (New, Continuing1, or Sequel2): New – This project addresses RFP 5 and 7.

Thrust(s): T2, T3

Industry Need and Project’s Potential Benefit to Member Companies: This project addresses the current need in industry to perform analysis and simulation on complex or very large systems.

Project Description: Blackbox macromodels have received increased interest in the signal and power integrity communities due to the growing complexity of networks used for computer and communications applications. These networks often exhibit frequency-dependent behaviors that are not easily captured by traditional circuit simulators such as SPICE. In the most common methods, two key steps are usually performed. First a model-order reduction (MOR) process is carried out to extract the multiport poles and residues of the network. The most commonly used and trusted approach for pole/residue extraction is the vector fitting method, which has proven to be robust and reliable (black arrows in diagram). In addition, passivity assessment and enforcement techniques have been made available to ensure viable and robust representation in the time domain. The computational burden in performing MOR is measured from the order of the approximation and the number of ports of the network. Systems with long interconnect delay will require higher orders, thus the need for delay extraction to reduce the computational complexity. Consequently, for complex systems involving a high number of ports, the task is still prohibitive.

The final step in the flow is to integrate the system into SPICE. Two methods are possible. 1) In the invasive approach, the SPICE source code is modified to include a recursive convolution algorithm that uses poles and residues and construct a stamp for the MNA matrix. 2) In the non-invasive approach, a circuit synthesis method is used to generate a SPICE netlist of circuit elements using the pole/residue information.

For the non-invasive approach, several efforts have addressed this synthesis such as [1], in which a Y-parameter representation is used to extract lumped circuit elements. Other techniques using S-parameters have been recently demonstrated [2]-[3] by the PI. The synthesis works as follows: for each pole/residue pair of a network parameter representing a port-to-port transfer function, an input circuit from a well-defined topology (lumped R, L, C) is excited. The response is constructed using a combination of dependent current sources. This synthesis process is driven by the poles and residues of the system, which must be extracted from a prior step. Pole/residue extraction (via vector fitting) and network synthesis have proven to be robust and reliable. However, for complex systems with large numbers of ports, these steps become very slow and may make the process intractable.

Preliminary work performed by the PI’s on using artificial neural networks (ANN) to assist macro-modeling (red path) using frequency domain data in the form of S parameters has proven to be encouraging. The ANN can be used to learn the nonlinear mapping between S-parameters and the underlying poles and residues. In addition, such a network can be made to adjust itself without knowledge of the reference poles and residues.
In addition, recent advances in machine learning (ML) for circuit design, indicate that ML techniques can be used to perform the synthesis directly from the S parameters, thus skipping the most time-consuming steps of pole/residue extraction and passivity enforcement (blue path). Further, a neural network might be trained to determine the optimum topology.

References

Progress to Date (if applicable): N/A

Work Plan (year 2019 only): To address the red path, our plan is to use a feed-forward neural network (FNN) architecture. This work can be extended to investigate deeper architectures to handle circuits with interconnects and extract the delays. Also, the SFNN being proposed here successfully enforces the realness and stability condition for the macro-model. There is however no guarantee that the predicted poles are passive. Post-processing with passivity assessment and enforcement is still required to ensure the model is usable for time-domain simulation. This could be treated directly during training by modifying the optimizer so that it includes the passivity constraint during the search for the minimum of the cost function. This will be the subject of future work to improve SFNN methods for MOR.

For the blue path, our plan is to use a machine learning approach to perform the synthesis. Since passivity is an important design requirement, the objective optimized during training should include a passivity-enforcing regularization term. Recent results on computationally feasible certificates for passivity (at least for low-order models) \[4\] will be used to design such a regularization term. In addition, restricted-complexity synthesis (limiting the number of reactive elements) \[5\] will be incorporated into the ML pipeline. These techniques were developed with mechanical systems in mind, but can be readily mapped to the electrical domain due to the well-known one-to-one correspondence between electrical (R, L, C) circuits and mechanical (spring, damper, inerter, circuits).

Our plan is to test devices with larger numbers of ports as well as network parameter data from a field solver to study the effect of size and complexity on the efficiency of the method. In all steps, validation with our standard MOR tools will be performed. Our efforts will first focus on developing and validating an ML-based synthesis tool for a two-port network. Upon successful trials, our plan is to test devices with larger numbers of ports as well as network parameter data from a field solver to study the effect of size and complexity on the efficiency of the method. In all steps, validation with SPICE simulation will be performed.

Related work elsewhere and how this project differs: Most of the machine-learning system identification and model-order reduction applications have come from the computational fluid dynamics (CFD) community which has been investigating the subject for over a decade. More limited work has been produced from the electromagnetics community which is just now starting to look at machine learning techniques for MOR

Proposed deliverables for the current year: 1) Node-JS based tool that will determine poles and residues and extract interconnect delay from S parameters using trained neural network with no passivity enforced. 2) Node-JS based tool that will perform circuit synthesis directly from S parameters with no passivity enforced.

Projected deliverables for Year 2 (if applicable): 1) Incorporate passivity enforcement into codes.

Budget Request and Justification: Support for two graduate students is being requested ($40,000), travel to attend conferences and review meetings and supplies. For a total with overhead of $55K

Start Date: 1/1/19 Proposed project completion date: 12/31/2020
I/UCRC Executive Summary - Project Synopsis

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Title:** Exploring unknown spaces for malicious additions using GoldMine

<table>
<thead>
<tr>
<th>Tracking No.</th>
<th>Project Leader: Shobha Vasudevan</th>
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<tbody>
<tr>
<td>P18-12</td>
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| Type: (New, Continuing?, or Sequel?) New | Thrust(s): T4 |

**Industry Need and Project’s Potential Benefit to Member Companies:** Cryptographic primitives and protocols in algorithms assume trustworthy hardware. Control and communication functions assume that hardware platforms and microcontrollers they use are resilient to attacks. However, hackers and US government reports have demonstrated a surge in various kinds of compromises in electronics used in critical and day to day application domains. These include backdoors, counterfeiting, reverse engineering, hardware Trojans, IP piracy and side channel analysis.

In the supply chain, a key manifestation of hardware Trojans meant to snoop, or tamper with the original design, is as additional circuitry in the design. The large uncharacterized space in the IC for possible Trojans makes checking for them a very hard problem.

**Project Description:** Typical verification/test techniques check for known good, specified behavior of the design. Intrusion and tampering detection, however, need techniques that can find unspecified extra behavior. The question that verification answers is “does the circuit do what it is intended for” while security needs to answer “does the circuit only do what it is intended for and nothing else?” We propose to develop a methodology to detect tampering or intrusion in the design and/or manufacturing process. Our previous research, GoldMine [1][2][3][4], combines machine learning algorithms with model based algorithms to explore design space. In GoldMine directed testing, we developed a feedback loop between machine learning and static analysis (formal verification). The machine learning, being an inductive inferencing engine, can guess design behavior from simulation data. For each guess, the formal verification engine, which is a deductive engine, validates if the guess is correct for all inputs. If the guess is not correct, it also provides an error trace. The error trace, when fed back to the machine learning component, along with correcting the error, makes new inferences based on the information introduced by the error trace. Each inference can then be checked by the formal verification engine again. This iterative interaction between a model based deductive engine that acts as a domain expert, and a data driven, statistical engine that makes intelligent guesses, is very powerful in our experience. We are able to infer complex, subtle and corner case behavior very quickly about the design, often surprising to humans.

In this work, we propose to apply this technology to the malicious circuit detection problem, *i.e.*, of inferencing unknown behavior, beyond what is supposed to be specified in the model.

For example, a single inverter in the design could be replaced by multiple, odd number of inverters, and the functionality would remain the same. An input/output based functional test could not differentiate between these two cases. Since our method involves a machine learning driven state space exploration, it will be able to navigate parts of the state space in an attempt to learn the model. We will investigate if the machine learning algorithms are able to explore the state space beyond the model specific correction offered by formal verification.

We plan to investigate a variety of machine learning algorithms including random forest, SVM, AdaBoost, and LASSO. Each of these algorithms will be interfaced with the GoldMine counterexample guided test refinement module. For each inference from the machine learning module, the formal verification module will validate the guess and provide a trace as feedback.

We will experiment with circuits that intentionally have additional circuitry placed in them, to enable detection.

Our experiments will be conducted first on RTL simulations, and then on FPGA implementations of the hardware. We will conduct two types of experiments. First, we will first train the machine learning to generate tests on the RTL design with static analysis driven feedback, using white box simulations. We will then add unspecified behavior to the design, and determine if machine learning algorithms are able to detect extra behavior than what they were trained for. If the tests generated on the malicious design are
different from the tests generated on the untampered design, we will be able to localize the functionality or location of the tampering.

Second, we will apply the machine learning algorithms with static analysis feedback directly to the design with malicious insertions, with no training phase. In this case, we will examine if the exploration of the machine learning algorithms is able to expose the additional malicious behavior during the process of test generation.

We will use the Trojan and trust benchmarks available in literature for our experiments [5]. These include insertions of Trojans in hard to detect, malicious or opportunistic locations at the system level (module and interconnects), design level (registers and wires), netlist level and physical layout level. We also plan to conduct a vulnerability analysis as a side effect of our learning based detection mechanism. GoldMine has an inbuilt ranking strategy for RTL design variables. This is based on importance, complexity in understanding, coverage etc. We can also add an "expectedness" criterion that ranks variables based on how likely the observed behavior is, when compared with base input probabilities from typical workloads. Unexpected behavior will be weighed higher in these rankings, providing visibility to previously unseen behavior. Human experts can analyze this further for design variations/bugs or maliciously inserted hardware.

References
3. Lingyi Liu, David Sheridan, Viraj Athavale, Shobha Vasudevan: Automatic generation of assertions from system level design using data mining. MEMOCODE 2011: 191-200

Work Plan (year 2019 only): 1. Experiment with current algorithms in GoldMine on RTL design simulations to determine the extent of unspecified behavior explored
2. Develop new algorithms in GoldMine that can interface and provide feedback to different types of static analysis information with specialized machine learning algorithms like SVM, AdaBoost and LASSO, as well as ensemble methods.

Related work elsewhere and how this project differs: There has been a surge in hardware security research for the past decade, especially in Trojan detection and mitigation in different parts of the supply chain[6]. To the best of our knowledge, the use of machine learning regulated by formal verification in detecting unseen behavior has not yet been studied.

Proposed deliverables for the current year: 1. Detection algorithms for malicious hardware insertions in RTL based on machine learning
2. Vulnerability analysis algorithms for analyzed benchmark circuits

Projected deliverables in Year 2 (if applicable): We will experiment with FPGA implementations of RTL designs, and investigate if insertions can be detected by the GoldMine tool suite.

Budget Request and Justification: $70,000
1 graduate student RA for 12 months, travel to conferences and collaborating companies

Start Date: 1/1/19     Proposed project completion date: 1/1/2020
Industry Need and Project’s Potential Benefit to Member Companies: Side-channel attacks are a major threat for the cyberspace. The best known attacks for quantum-secure encryption, however, cannot yet scale to practical devices. This project illustrates how they can using machine learning and adaptation of an existing attack. This proposal is responding to research need 6, **Machine learning in Secure and Trusted Designs**

**Project Description:**
The primary purpose of this project is to enable single-trace power side-channel attacks on post-quantum key-exchange protocols using machine learning and to quantify the strength of timing obfuscation defenses against these attacks. The central questions we address are can machine-learning approaches provide stronger attacks compared to the conventional ones in the context of lattice-based cryptosystems and to what extend can obfuscation methods hide the vulnerability.

Public-key cryptosystems of today are vulnerable to quantum cryptanalysis because they rely on problems such as integer factorization and (elliptic curve) discrete logarithm that can be efficiently solved by a quantum computer in polynomial time. Post-quantum cryptography seeks alternative, quantum-resistant cryptographic systems that can survive the quantum threat. These cryptosystems are still classical algorithms that execute on classical computers but they rely on different problems that so far are not vulnerable to quantum cryptanalysis. Among potential proposals, lattice-based cryptosystems have been a predominant class that was even deployed in commercial products. Although the theoretical cryptanalytic strength of lattice algorithms are thoroughly being analyzed, practical attacks on their implementation are largely unexplored. Side-channel attacks are a broad category of such attacks that can extract secret cryptographic keys by analyzing algorithm’s execution behavior in a computing device.

Power-based side-channel attacks are a fundamental threat for CMOS technology because switching activity (i.e. power consumption) is inherently data dependent. Therefore, when the secret key is being processed, there is some correlation between its value and the power measurement. This correlation is extracted conventionally through Differential Power Analysis (DPA) requiring repeated measurements to apply a covariance or difference-of-means test. A straightforward adaptation of this attack is infeasible for key-exchange protocols because the secret key changes after each execution—i.e., there exists a single power measurement to analyze when attacking a key.

The project leader of this proposal recently showed the first successful side-channel attacks on lattice-based key exchange protocols that extracts the entire secret key form a single power measurement trace. The proposed method applies a Horizontal DPA that combines small correlations observed “within” a single execution (Fig. 1 (a)). The underlying lattice-arithmetic—matrix and polynomial multiplications—indeed has a large number of intermediate computations that depend on the same part of the secret key, e.g., a secret-key coefficient is multiplied with all coefficients of the other polynomial. This attack breaks the implementation of Frodo (CCS’16) and NewHope (USENIX’16) key-exchange protocols.

Although the proposed attack is successful, its application is limited to a small subset of implementations. The critical deficiency in the attack procedure is under utilizing the information available in the correlation trace (Fig. 1 (b)). The attack focuses on a single point in time where the maximum leak occurs and estimates the correct key purely based on that information omitting other data points (Fig. 1 (c)). As a result, the proposed attack can only succeed on a fully-serialized hardware design that processes a small chunk of information (of 8-bits) at a clock cycle (Fig. 1 (d)). A parallelized hardware, by contrast, will add algorithmic noise and reduce the number of distinct tests, rendering the attack useless.

Our hypothesis is that machine-learning classifiers can improve the best-known attack and can therefore extend the threat towards microcontroller-based designs. We furthermore argue that, in this application context, a machine-learning attack can even surpass the template attack, which is the best conventional method. It has been recently simulated that Random Forest classifiers can theoretically outperform template attacks when the attackers only have access to few traces each with a large number of data points [2]. Post-quantum key-exchange protocols using long lattice arithmetic computations and one-time keys are unique instances of this scenario. Therefore, if successful, our proposal will be the first practical demonstration of machine-learning classifier superiority over prior methods that have been used for the last two decades.
we will train more powerful classifiers based on neural networks and compare their success to conventional attacks.

A straightforward mitigation of power side-channel attacks is inserting random dummy states during cryptographic execution. While these countermeasures work for DPA/template-style single-trace attacks, neural networks have a potential to thwart such simple defenses. Indeed, neural network classifiers such as the Long-Short Term Memory (LSTM) is known for being robust to temporal noise, hence are used in time-series classification with noisy data. Later in the project, we envision to apply random delay insertion techniques for defense and analyze their effect on the classification performance against LSTM-based attacks vs. conventional techniques.

Work Plan (year 2019 only): The 2019 work plan is to realize parallel implementations of key-exchange protocols, demonstrate machine-learning side-channel attacks, and compare it with the DPA/template attack results.

Related work elsewhere and how this project differs: The project leader demonstrated the only successful side-channel attack on lattice-based key-exchange protocols, which is limited to 8-bit serial hardware implementations [1]. Through machine-learning classifiers, this project will enable the attack on a broad class of architectures. The potential of machine-learning for side-channel attacks has been theoretically hinged by Lerman et al. [2]. We will reveal its practical value by demonstrating in the context of post-quantum key-exchange protocols.


Budget Request and Justification: $54.5K/year, including support for 1 student ($30K salary & benefits, $17K tuition), $4K travel, and $3.5K indirect costs.

Start Date: 1/1/19

Proposed project completion date: 12/31/2020
### I/UCRC Executive Summary - Project Synopsis

**Date:** 08/17/2018

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Title:** Design Space Exploration using DNN

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<tr>
<th>Tracking No.:</th>
<th>Project Leader:</th>
<th>Co-investigator(s):</th>
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<tr>
<td>P18-16</td>
<td>Prof. Madhavan Swaminathan</td>
<td>Collaborations with Prof. Paul Franzon and Prof. Rhett Davis (NCSU), Prof. Elyse Rosenbaum (UIUC) and Prof. Sungkyu Lim (GT)</td>
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**Type:** (New, Continuing, or Sequel)  
New

**Thrust(s):** T2/T4

#### Industry Need and Project's Potential Benefit to Member Companies:
Designing advanced semiconductor manufacturing process brings area, speed, power and other benefits but also new performance challenges as a result of the pure physics of running current through tiny wires. Often times there are post tape-out escapes both at the silicon and packaging levels due to inadequate analysis at an early design stage. This sometimes is due to lack of time or poor assumptions made by the designer which may be inaccurate. We address these challenges in this project by focusing on early Design Space Exploration (DSE). Such a solution we believe would be applicable to various levels in the system hierarchy.

**Research Need:** Corner tightening and LLE.

**Project Description:** The Problem: Various process parameter like Local Layout Effects (LLE) etc., have critical impact on design, and introduce variability to circuit design, and significantly impact device performance as well as characteristics. These effects need to be accounted for during the earliest stages of design when the chip architect is crafting the architecture, else the design may not meet the design specifications. Predicting the performance of interconnects and other structures at an early design stage is still an un-tackled problem. Predicting the output is particularly difficult because of the non-linear interactions among input parameters that are either augmented or weakened when combined, undiscovered LLE effects, dataset noise etc. The interacting effects among inputs, bring extra challenges on the output design specifications, like LLE effects cannot be inferred from calibration macro set etc. Often times the design space needs to be restricted since simulations take a long time or predictions are inaccurate due to simple models. The design space gets restricted because of the problem of extrapolating outputs far from the experimental values. This is due to the nonlinearity of the response and the anomalous behavior of high dimensional statistics. For example doing design space exploration (DSE) using say higher order Taylor expansion and others fail miserably as they cannot capture the nonlinearity and high dimensionality of the problems involved [1]. Added to this list is the problem of simulation using the physics based model EM solver. The EM solvers are computationally expensive and requires high computational framework like parallel machines. The need of the hour for the circuit designer is fast and accurate deep learning techniques to model the LLE residual instead of replacing the entire circuit models and extracting the features of LLE. The DNN has the extraordinary ability to generalize concepts from the data and can predict accurately over the new hardware designs, on which it has not been trained [4].

**Proposed Solution:** In this project we propose the use of Deep Neural Networks (DNN) to model LLE residual on the fly to predict the compact modeling calibration macros and compare predictions with hardware results. The DNN search for the best solution space of calibration macros will be from samples in a variety of directions in parallel. Based on the data samples, the DNN discards low-value optimization directions from its search space and chooses the most valuable optimization directions to progress towards a solution. Our proposed DNN, will use distributional optimization from samples (DOPS), and will circumvent the difficulties to model the objective function for example LLE residual, eye diagram etc. on demand [1, 2]. The DNN we propose “learns to optimize” from the samples only, without a predefined objective function as most traditional machine learning algorithms do. For example, in the problem of modelling the LLE residual on demand, the goal is to choose an “appropriate datasets” of calibration macros such that, we maximize objective function, which the circuit designer has given before. Formulating targeted objective functions for a circuit designer (for complex circuits) in most cases can be impossible. Our proposed DNN formulates the objective function from the data and chooses those samples that maximizes the objective function and discards others. Our proposed DNN model learns from the data by an innovative procedure called “distributional optimization from samples (DOPS)” [3, 4] that gets rid of noise in the datasets by squeezing the information through a bottleneck, while retaining only the features most relevant to generalization concepts as shown in Figure 1. This not only gives generalization over the new hardware, but also gives the necessary information of features required like additional LLE features, the distribution...
invariance of input/output for generating RLGC models etc [3]. Once the DNN models are generated, we can apply earlier work done through CAEML for optimization [5].

Once the DNN models are generated, we can apply earlier work done through CAEML for optimization [5].

Figure 1: (a) Deep Learning using Information Bottleneck Pipeline for Design Space Exploration; (b) An example application where the interconnection dimensions are predicted during the routing phase to achieve 16Gbps performance with minimum jitter and maximum eye opening.


Progress to Date (if applicable): We have built our DNN on the Tensorflow framework and trained it by an Amazon EC2 instance using batch processing. Each of these Amazon EC2 instances are created on the fly for training and is deleted on completion. We have applied it to frequency response of RLGC parameters of transmission lines.

Work Plan (year 2019 only): The work plan consists in developing a scalable Deep Neural Network model (DNN) using the information bottleneck for predicting the frequency response. This requires building a scalable Deep Neural Network model (DNN) in Tensorflow framework in distributed cloud framework. Then we validate our DNN prediction with outputs from a physics based EM solver and circuit simulators for different circuit configurations and instances along with optimization.

Related work elsewhere and how this project differs: We are unaware of work in the area of DSE.

Proposed deliverables for the current year: 01/19-04/19: Development and implementation of DNN with Information Bottleneck. 05/19-12/19: Application and validation of DNN predictions with physics based EM solvers and circuit simulators on designs from industry.

Projected deliverables for Year 2 (if applicable): 01/20–12/20: Development of a mapper and application to industrial strength problems.

Budget Request and Justification: Year 1: $75328 (1 full time GRA for 12 months; 25% Post Doc; $5K travel); Year 2: $77416 (1 full time GRA for 12 months; 25% Post Doc; $5K travel).

Start Date: 1/1/19  Proposed project completion date: 12/31/2020
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