Welcome & Introductions

8:00-8:15 am
Welcoming Remarks
Paul Franzon, NCSU CAEML Site Director

8:15-8:30 am
Introductions
Dale Becker, IAB Chair
Quick Overview of Day’s Activities

Jill Peckham:

Review of the meeting agenda
IUCRCs and LIFE forms
Dee Hoffman
I/UCRC Evaluator for NSF
8:30 - 9:30 am
NSF & Assessment Coordinator Introduction

Dee Hoffman, PhD

Center for Advanced Electronics
Through Machine Learning

I/UCRC IAB Meeting #3
October 2017
Agenda

- Brief IUCRC Update
- Assessment Coordinator's Role
- L.I.F.E. = Level of Interest Feedback Evaluation
Who we are

**NSF’s Vision** - NSF’s vision is a nation that creates and exploits new concepts in science and engineering and provides global leadership in research and education

- ~$7.3B Budget

- 217 Nobel Laureates supported

- Overall: 350,000 researchers, postdoctoral fellows, trainees, teachers, and students supported

- ~400 startups/small businesses funded each year
The Industry University Cooperative Research Program: I/UCRC

40 Years of Building Research and Innovation Capacity

- First Center Proposals Received in 1972
- First “Experimental” Awards Made in 1973

Cooperatively Defined and Shared, Sector Precompetitive Research

“Determine effective ways of stimulating non-Federal Investment in R&D and of Improving the application of R&D results.”*

*President’s message to the Congress on S&T, March 16, 1972
The Industry-University Cooperative Research Centers (IUCRC) Program

Mission:
• To contribute to the nation’s research infrastructure base by developing long-term partnerships among industry, academe and government
• To leverage NSF funds with industry to support graduate students performing industrially relevant research

Vision:
• To expand the innovation capacity of our nation’s competitive workforce through partnerships between industries and universities

Cooperatively Defined and Shared, Sector Precompetitive Research

1980’s 1990’s 2000’s 2010’s

40 years of fostering and growing long-term partnerships among industry and academe based on shared value
What is an IUCRC?

- A Partnership: A mechanism to enable industrially-relevant, pre-competitive research via a sustained partnership among industry, universities, and government.

- Centers bring together
  1. IUCRC Sites (Academic Institutions)
     - Faculty and students from different academic institutions
  2. IUCRC Industry Members
     - Companies, State/Federal/Local government, and non-profits

- Focus
  - Perform cutting-edge pre-competitive fundamental research in science, engineering, technology area(s) of interest to industry and that can drive innovation and the U.S. economy.
  - Members guide the direction of Center research through active involvement and mentoring.
IUCRC Model: Core elements

- Membership fees for participation
- Semi-annual meetings for stakeholders
- Industrial Advisory Board (IAB)
- Projects are selected via voting and consensus
- Research results are shared with all members
NSF’s Role

Facilitate a Center environment in which long-term relationships between industry and academia can thrive.

- **Cooperative Agreement & Operational Framework**
- **Provide 40+ year experience managing I/UCRCs**
- **Franchise of centers for collaboration**
- **Provide networking opportunities**
- **NSF Award – Seed Funding Opportunities/Oversight**
NSF’s role

• Supports development and evolution of IUCRCs

  • Funding to support administrative operations
  • Structure and operational model
  • Best practices from 40 years experience
The I/UCRC Model: Linking Industry to Fundamental Research

I-U Cooperative Research Domain

Academic Fundamental Research

Sector Pre-Competitive Research

Industry Sector-Competitive Research

• User-Inspired Fundamental Research
• Industrially relevant
• Jointly Funded
• Non-exclusive IP access

I/UCRC Domain

Ideas, People
I/UCRC Nucleus: A Cooperatively Defined, Funded & Shared Research Portfolio

Requires trust be built in the model, and between all partners in the center.
I/UCRC Membership Agreement

- Parties to Agreement, University, IAB members, and the I/UCRC
- Annual membership fee structure
  - Patent rights held by university with royalty free, non-exclusive rights to Center members.
  - Companies wishing to exercise rights to a royalty-free license pay for the patent application.
  - If only one company seeks a license it may obtain an exclusive fee-bearing license.
- Compliance with chapter 18 of title 35 of the United States Code, commonly called the Bayh-Dole Act
- Publication delay policy.
- Industrial Advisory Board – one representative from each company per membership.

- All Members sign the agreement upon Center Award
- ONE center, and ONE membership agreement form
What Value does an I/UCRC Offer?

Value to Industry Members
- High value research projects
- Investment leveraging
- Sector networking, learning from industry peers and customers
- Access to intellectual property
- Pre-publication research access
- Access to students
- Access to faculty & facilities

Value to Center Institutions
- New research and education dimensions
- Student training, recruitment and placement
- Supplemental grants opportunities
- Trusted relationships with industry
- Increase in industry understanding
- Means to achieve institutional mission.

Outcomes from a cooperatively defined and managed, portfolio of precompetitive research.
76 I/UCRC Centers and Growing!

6 International Sites
Belgium, Finland, Germany, India (2)

**NSF Funding**
- ~$20.6M in Program Funding
- ~ 6:1 Leveraging of NSF funds

**Members**
Close to 875 unique industry members involved (17 on Average per Center)
~ 47:1 leveraging of member funds

**Students**
Over 2500 students engaged (nearly 30% of graduates are hired by members on an annual basis)

**Senior Research Investigators**
Close to 1100 senior research investigators involved (~17 on average involved per center)
2016 Industry-Nominated I/UCRC Technology Breakthroughs – a Compendium

What will be this center’s Impact Stories?!

Over 1400 Publications in ’13, 248 co-authored w/Members

National Science Foundation I/UCRC

Contacts

Program phone: (703) 292-8383   Program email: iucrc@nsf.gov

ENG/BIO/GEO:

Prakash Balan, ENG Program Director, pbalan@nsf.gov

CISE/Forensic/Brain:

Dmitri Perkins, CISE Program Director, dperkins@nsf.gov
Thyaga Nandagopal, CISE Program Director, tnandago@nsf.gov
Rita Rodriguez, CISE Program Director, rrodrigu@nsf.gov
Alex Schwarzkopf, Consultant, aschwarz@nsf.gov

Carl Anderson, MIPR/IAA Program Specialist, cnanders@nsf.gov

Planning/IAB Mtgs Master Calendar, iucrctravel@nsf.gov

for more information: http://www.nsf.gov
and: http://www.nsf.gov/eng/iip/iucrc

Note: The best way to contact us is via e-mail. Avoid voicemail if possible
Many are on the road frequently
Evaluator & LIFE Agenda

- IUCRC Evaluation Program
- Evaluator's Role
- L.I.F.E. = Level of Interest Feedback Evaluation
IUCRC Evaluation Program: Goals

1. Document IUCRC accomplishments and outcomes
2. Assure center fidelity to the I/UCRC Model
3. Share options and examples for IAB meeting elements
Level-of-Interest Feedback Evaluation
L.I.F.E.
Level-of-Interest Feedback Evaluation (L.I.F.E.)

- Feedback for Scientists on projects
- Reviewed in IAB - basis For Dialogue
- Not voting mechanism – multiple members of one company may complete
- Way of capturing feedback and responses
- Poster Session is a great place to get detailed questions answered
- Hand out in the folder on how to access
Level-of-Interest Feedback Evaluation (L.I.F.E.): Process

• At the end of each project presentation members rate interest or progress & comment on projects
• PIs respond on LIFE site
• IAB reviews
Level-of-Interest Feedback Evaluation (L.I.F.E)

Two Options

- On-line
- Paper

Preference!!!
Level-of-Interest Feedback Evaluation (L.I.F.E.): Process

www.iucrc.com
Open Meetings

The following listing of meetings is within a +/- 30 day range:

<table>
<thead>
<tr>
<th>Date</th>
<th>Center Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>October 5th, 2017</td>
<td>CenTire</td>
</tr>
<tr>
<td>October 12th, 2017</td>
<td>CAEMI</td>
</tr>
</tbody>
</table>
Password: CAEMLFall2017
Industry members select Industry

If you select Industry you will next see this …
## CAEML () - October 12th, 2017

### IAB Feedback

#### Index of Projects

<table>
<thead>
<tr>
<th>Project Phase</th>
<th>Project Title</th>
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<tbody>
<tr>
<td>Update</td>
<td><strong>Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems</strong>&lt;br&gt;- A. Cangellaris and M. Raginsky ()</td>
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<td>1A2</td>
<td>Evaluate Project</td>
<td>Summary</td>
</tr>
</tbody>
</table>

Designated member representative *(one per member)* please complete the [Member Benefits Inventory](#).
Industry / University Cooperative Research Centers
Member Benefits Inventory

The goal of this survey is to identify and document the Center membership benefits your organization has received during the current membership year. This information is helpful for center evaluation. It may also help your organization characterize the benefit of your investment in the center, and justify continued membership. Upon completion of the survey, you may download a copy of your organization’s benefit inventory for internal use.

Please select your Center’s name from the list below.

Advanced Electronics through Machine Learning
### CAEML () - October 12th, 2017

**IAB Feedback**

- **Index of Projects**

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*Designated member representative (one per member) please complete the Member Pulse Survey*
Level-of-Interest Feedback Evaluation

New/Proposals

- Level of Interest
  - Very interested
  - Interested
  - Interested with change
  - Not interested

-----------------------------------------

- Abstain (outside my group's ability to evaluate)

- I've already rated - providing additional comments
L.I.F.E. Feedback Evaluation

Current Updates

Level of Interest
- Great progress
- On course
- Needs change
- Off course

Abstain (outside my group’s ability to evaluate)
I’ve already rated - Providing additional comments
Please provide any comments, questions or suggestions you have about this project, the progress made, and technical or implementation issues.

**Comments:**

Provide any comments about this project here.

**(optional)**

**Question:**

Provide any questions about this project you would like the PI to address.

**Suggestion:**

Provide any suggestions you have for improving this project or making it more relevant to you needs or interests.
L.I.F.E. Comments & Questions

- Offers of help, support, equipment, etc.
- If needs change – What is the change?
- Similar work elsewhere
- Suggestions
- Pre-competitive applications
- Benefits and Relevance
- If current or ending project: What went well – What would have made better - Recommendations for improvements in research or in aspects of project such as design, budgeting, communication, teamwork
But someone may ask who said it!
### CAEML () - October 12th, 2017

#### IAB Feedback

#### Index of Projects

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</tbody>
</table>
If you select [Faculty] you will next see this …
Instructions for PIs:

By selecting "Response to comments" on the following page next to your project you will be able to respond to specific comments provided by IAB members. Simply write a reply in the text box that is provided, enter your name and select "Submit Response" when done. Multiple PIs can submit comment. Your reply and name will be visible to all who access the site and will be debriefed at the IAB session.

Please note:

- Only provide replies for your project
- Do not feel obligated to reply to every comment (e.g., "great project" probably doesn't require a reply)
- Be brief and to the point in your replies: less is more

Continue to Response Page
For your project, select “Respond to Comments”

<table>
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</tr>
</tbody>
</table>
No special characters! *## etc.!

CenTire - October 5th, 2017

<< Previous  (01) Multi-scale modeling  Next >>

Project Update
Project Name: (01) Multi-scale modeling of tire wear  
Project PI: Taheri with Emami, Vadakkeveetil & Su (VT)

Progress Ratings
Great progress - 0  
On course - 0  
Needs change - 0  
Off course - 0  
Abstain - 0  
Additional Comments - 0

PI Summary Response

Comments - 0  
Questions - 0  
Suggestions - 0

Page 1 of 1

Comment

Name *Names will be visible by everyone

Required

SELECT SUBMIT AFTER RESPONDING TO each page of comments.

Multiple PI’s/Students can respond to a project.
When done with comments go back up to the links in blue and select questions – then respond.....
<table>
<thead>
<tr>
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<td>1A2</td>
<td>Respond to Comments</td>
<td>Summary</td>
</tr>
</tbody>
</table>
Level of Interest

Very Interested - 0
Interested - 1
Interested with Change - 0
Not Interested - 0
Abstain - 0

Here’s an example of what we might see during review.

Summary of PI Responses

Dee’s Response: This project has received great support from the mentors. We do need a firm meeting time however.

Question

▶ Is there any IP we should be aware of?
  Response 1: None at all. This is entirely original. -Dee

Suggestion

▶ We need more mentors.
  Response 1: Please tell me who this is! -Dee

Comment

▶ This is a great project!
  Response 1: Thanks! -Dee
Level-of-Interest Feedback Evaluation (L.I.F.E.): Instructions

Paper Option

1. Find L.I.F.E. Form in notebook with project name
2. Mark Level of Interest, add comments
3. Give paper L.I.F.E. Form to Evaluator & repeat...
### IAB Review – The Discussion Leader Role

<table>
<thead>
<tr>
<th>Project:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Summary: Provide a 2-3 minutes summary of the themes you noted in the LIFE for this project: critical IAB likes, issues, concerns, desired changes, questions, etc.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NOTES – Use to make note of things you might want to highlight</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Comments./Questions/Concerns</td>
<td>Suggestions/Changes</td>
</tr>
</tbody>
</table>
State of the Center

Elyse Rosenbaum
University of Illinois at Urbana-Champaign
9:30 - 9:45 am
The center’s goal is to enable fast, accurate design and verification of microelectronic circuits and systems by creating machine learning algorithms to derive models used for electronic design automation.

By speeding up the design and verification of microelectronic circuits and systems, CAEML will reduce development cost and time-to-market for manufacturers of microelectronic products, and will enable the development of optimized products, e.g. for low-power, high-reliability or security.
Research Thrusts and Research Projects

• **Unifying theme:** Better electronic designs and design automation through machine learning

• **Thrusts:** *Theory, devices, and systems*

• **Theory**
  - Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems (1A6, in progress)
  - Security-centric Synthesis and Optimization for Trusted Hardware Design (2A1, new proposal)
  - Causal Inference for Early Detection of Hardware Failure (2A6, new proposal)

• **Devices**
  - Intellectual Property Reuse through Machine Learning (1A2, in progress)
  - Machine Learning to Predict Successful FPGA Compilation Strategy (2A4, new proposal)
Research Thrusts and Research Projects, cont’d

- Applying Machine Learning to FPGA Design (2A5, new proposal)
- Applying Machine Learning to Back End IC Design (2A7, new proposal)
- Applying Machine Learning to Design Rule Checking (2A8, new proposal)

• Systems
  - Behavioral Model Development for High-Speed Links (1A5, in progress)
  - Models to Enable System-level Electrostatic Discharge Analysis (1A6, in progress)
  - Optimization of Power Delivery Networks for Maximizing Signal Integrity (1A7, in progress)
  - Machine Learning for Trusted Platform Design (2A2, new proposal)
  - Causal Inference for Building Trust in Platform Designs (2A3, new proposal)
Center Membership
Accomplishments Year 1

• First center meeting (kick-off) held Oct 2016 at UIUC
  10 member companies, 1 guest company rep., 9 center faculty
  8 project proposals presented, 6 received funding
• Memorandums of Understanding between the three universities were completed
• Operations Manager hired Jan 2017
• Second Semiannual Center meeting held April 25 & 26 at Georgia Tech
  Progress Reports on all research projects, in depth discussions of by-laws and research roadmap
• Research projects started Jan 2017
  o 1 journal article, 4 conference papers and 1 invention disclosure
  o And year 1 hasn’t yet ended ….
• NSF annual report submitted July
• Significant effort on recruitment – now have 12 members
  o Appears likely that number will soon increase further
• Engaged 18 students in research on the application of machine learning to EDA


A black box optimization algorithm: Two Stage Bayesian Optimization.

Hakki Mert Torun & Madhavan Swaminathan, Georgia Institute of Technology Research Corp.
Education

Introductory Machine Learning Tutorial by Max Raginsky, March 14, 2017

Machine Learning Assisted IC Design, Modeling, Optimization and IP Reuse webinar by Weiyi Qi August 31, 2017
Outreach to Prospective Members Since April 2017

Elyse

- May 7. Presentation at the International Electrostatic Discharge Workshop (IEW). *Machine Learning for EDA*
  - Attendees from Intel, ST Microelectronics, ARM, and others
- May 24. Webinar for **GlobalFoundries**. *Electronics Modeling and Design Optimization with Machine Learning*
- Introduced CAEML to Apple, Cirrus Logic, and PDF Solutions in presentations given July 2017.
Outreach to Prospective Members: Since April 2017

Paul

- Visits to Sandisk (Western Digital), Draper Labs & Mentor Graphics (Siemens)
- May 13 Webinar for DARPA. Machine Learning and EDA.
- June 5. Webinar for GlobalFoundries. Machine Learning and EDA.
Outreach to Prospective Members
Since April 2017

Madhavan

  - With Hakki M Torun, Anto K. Davis, Mohammad L.F. Bellaredj
CAEML Students’ Summer 2017 Internships

Bowen Li (NCSU) - HPE
Thong Nguyen (Illinois) - Qualcomm
Weiyi Qi (NCSU) - Samsung
  Subsequently joined Samsung after Ph.D. completion in Fall
Yi Wang (NCSU) - HPE
Huan Yu (GT) - Cadence

Zaichen Chen (Illinois) - Texas Instruments, Dallas
Billy Huggins (NCSU) - Northrop Grumman
Xinying Wang (Illinois) - Ansys
Jie Xiong (Illinois) - Global Foundries
Alan Yang (Illinois) - Rincon Research Corp
Opportunity for student recruitment

CAEML students want summer internships at the member companies!

We will create a student resume “book” and distribute it to the IAB reps by November 10 to assist you in identifying prospective interns.

If your mentors are already working with CAEML students on projects, they can recruit those students now for next summer.

Some of the CAEML students have already received 2018 internships offers from outside companies.
<table>
<thead>
<tr>
<th>ID</th>
<th>Project Title</th>
<th>Project PIs</th>
<th>Planned Duration (yrs)</th>
<th>Start</th>
<th>Year 1 allocation ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1A1</td>
<td>Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems</td>
<td>Raginsky, Cangellaris</td>
<td>3</td>
<td>1/1/17</td>
<td>96,000</td>
</tr>
<tr>
<td>1A2</td>
<td>Intellectual Property Reuse through Machine Learning</td>
<td>Franzon, Floyd</td>
<td>2</td>
<td>1/1/17</td>
<td>89,200</td>
</tr>
<tr>
<td>1A4</td>
<td>Design Rule Checking with Deep Networks</td>
<td>Franzon, Davis</td>
<td>1</td>
<td>1/1/17</td>
<td>58,200</td>
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<tr>
<td>1A5</td>
<td>Behavioral Model Development for High-Speed Links</td>
<td>Swaminathan, Franzon, Schutt-Aine</td>
<td>2</td>
<td>1/1/17</td>
<td>166,182</td>
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<tr>
<td>1A6</td>
<td>Models to Enable System-level Electrostatic Discharge Analysis</td>
<td>Rosenbaum</td>
<td>2</td>
<td>1/1/17</td>
<td>63,746</td>
</tr>
<tr>
<td>1A7</td>
<td>Optimization of Power Delivery Networks for Maximizing Signal Integrity</td>
<td>Swaminathan, Ji</td>
<td>2</td>
<td>1/1/17</td>
<td>76,500</td>
</tr>
</tbody>
</table>
# Financial Overview

## RESEARCH ACCOUNTS

Year 1 Income from Corporate memberships
- 12 members @$50k  
  $600,000

Year 1 allocated for research projects  
$549,828

Year 1 research account carryover  
$50,172

Year 2 projected funds from corporate memberships
- 12 members @$50k  
  $600,000

Available for allocation at this meeting  
$650,172

Amount needed to continue current projects  
$469,057

Balance  
$181,115
Financial Overview

ADMINISTRATIVE ACCOUNTS - Illinois

Income from NSF (2 yrs) $300,000.00

Expenses to date 77,165.91

- salaries $38,050.94
- travel $9,734.84
- misc exp $868.69
- indirect costs $28,511.44

Balance for remaining thru 7/31/18 $222,834.09
## Financial Overview

### ADMINISTRATIVE ACCOUNTS – Georgia Tech

- **Income from NSF (2 yrs)**: $300,000
- **Expenses to date**: $140,136
  - Salaries: $51,744
  - Fringe: $15,053
  - travel*: $7,708
  - misc exp: $17,456
  - subcontract: $0
  - indirect costs: $48,143

**Balance for remaining thru 7/31/18**: $159,863

*travel encumbrances not included*
## Financial Overview

**Administrative Accounts - NCSU**

<table>
<thead>
<tr>
<th>Description</th>
<th>Amount</th>
</tr>
</thead>
<tbody>
<tr>
<td>Income from NSF (2 yrs)</td>
<td>$300,000</td>
</tr>
<tr>
<td>NSF REU for Veterans Supplement</td>
<td>$8,000</td>
</tr>
<tr>
<td>Expenses to date</td>
<td>$51,440</td>
</tr>
<tr>
<td>salaries</td>
<td>$5,861</td>
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<tr>
<td>travel</td>
<td>$8,242</td>
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<tr>
<td>misc exp</td>
<td>$19,850</td>
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<tr>
<td>indirect costs</td>
<td>$17,486</td>
</tr>
<tr>
<td>Balance for remaining thru 7/31/18</td>
<td>$256,559</td>
</tr>
</tbody>
</table>
Director’s Concluding Remarks

- Special welcome to new faculty
- Industry reps: your active and enthusiastic assistance can help us achieve wide engagement with your company
Closed Door IAB Meeting

Attendance restricted to IAB and NSF

9:45 - 10:45
Closed Door IAB meeting

IAB and NSF only in this room please.

Everyone else may adjourn next door.

Please be back in this room to resume promptly at 10:45 am
Presentations will be in the Quad Chart format requested by the IAB. Specific times are outlined in the agenda.

Additional technical details on each project will provided (by the graduate students) during the lunch-time poster session

Out of respect to all the presenters and attendees, we plan to stay on schedule with project reports.
LIFE Forms on Year 1 projects

Five minutes are allotted at the end of each presentation for LIFE form completion.

If you start your LIFE form at that time, you will be required to rate the project before you close the form. That rating cannot be changed later, although you can go back in and make further comments.

Alternatively, you can take notes during the presentations but not complete the LIFE form until after the lunch poster session.

Time has been allocated for this.
1A1 Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems

PIs: M. Raginsky & A. Cangellaris
Students: J. Laurel, X. Ma, S. Markowitz

Year 1 Allocation $96,000
October 12, 2017
Project Definition

- Objective: theoretical foundations and modular algorithms for ML-driven design, simulation, and verification of high-complexity, multifunctional electronic systems.
- Relevance to Industry: improve time-to-market and mitigate overly pessimistic designs using ML and probabilistic modeling.

Results and Significance

- Application of VAE to probabilistic generative modeling of interconnect response in the presence of manufacturing variability, with relaxed functional constraints.
- Stability-inducing regularization for RNN models of circuits that compose well with circuit simulators like Verilog-A (synergy with 1A6).

Progress

- Implementation in Python (Theano + Keras), automatic generation of Verilog-A netlists from learned RNN models.
- Implementation in Matlab and Python (Tensorflow + Keras), VAE-based probabilistic generative modeling of S-parameters for interconnects with manufacturing variability

Future Outlook

- Use ideas from optimization and nonlinear system stability to inform the design of learning algorithms and component/system verification tools.
- Stochastic behavioral models of components and systems = Probabilistic Programs
Objectives and Experimental Plan

- Phrase behavioral system modeling (both during learning and during simulation) as **probabilistic programs**:
  - PPs consist of deterministic transformations (nominal device models), random variable generators (to capture noise and component/process variability), and probabilistic conditioning (to capture constraints or relations among internal and external variables).

- **Probabilistic programming approach will allow us to develop robust and mathematically sound techniques for capturing all sources of noise and variability in behavioral models**:
  - Using formal verification tools, we can quantify the concentration of typical system behavior around the mean or median nominal model. This will pave the way for more efficient and meaningful predictive EMI analysis at the system level.
Milestones and Deliverables

• **Milestones**
  o Develop a theoretical and algorithmic framework for modular ML on both component level (using probabilistic programs to sample behaviors of components) and system level (using behavioral system theory to specify interconnections and circuit constraints that can be automated using a probabilistic program compiler).
  o Identify test structure for system-level EMI modeling.

• **Deliverables**
  o Design and characterization of each element of the ML pipeline as a probabilistic program, including tools for uncertainty quantification in behavioral models.
  o Report on the application of probabilistic modeling to expedite EMI modeling and simulation of realistic electronic systems.
## Budget Request

<table>
<thead>
<tr>
<th>Category</th>
<th>Number</th>
<th>Cost (per year)</th>
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1A2 IP Reuse through Machine Learning
PIs: P. Franzon & B. Floyd
Students: Yi Yang, Weiyi Qi, and Weihu (Fred) Wang
Year 1 Allocation $166,182
October 12, 2017
## Project Definition

- Automatic reuse of circuit IP in moving IP between technology nodes
- Fast optimization of custom circuit blocks
  - Topology fixed
- Improves productivity for custom circuit designers

## Results and Significance

- Bayesian optimization produced better design result than human designer
- Optimization 3x faster than Genetic Optimizer

## Progress

- Code capturing Bayesian Optimization process in SUMO almost ready for distribution
- Demonstrated on Balun and on Power Amplifier
- Journal paper in preparation

## Future Outlook

- Apply code to mixer
- Extend to SerDes circuit
- Improve capability with neural network inverse modeling
Objectives and Experimental Plan

- Apply code to mixer
- Extend to SerDes circuit
  - SerDes circuit will also be applied to 1A5
- Improve capability with reverse neural network modeling
  - Model building itself can be used to generate feasible designs
    - Fits valid inputs to specified outputs, e.g. by taking an inverse of the activation function for a hidden layer, dividing it by the sum of incoming weights, and multiplying it by the weight of the first layer.
Milestones and Deliverables

- March: Mixer complete
- June: SerDes design complete
- Sept: Inverse Neural network feasibility established
- Dec: Applied to SerDes
# Budget Request

<table>
<thead>
<tr>
<th>Category</th>
<th>Number</th>
<th>Cost (per year)</th>
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1A4 Design Rule Checking with Deep Networks

PIs: P. Franzon & W. Davis
Students: Tanmay Lagare, Arpit Jain, Madhura Kulkarni, Divya Sardana, Somal Chaudhary, Luis Francisco, Billy Huggins
After Award, IAB encouraged us to pursue three projects in this one year, one student investigative project. We worked MS student resources to do this.

- DRC with Deep Networks
- Back end design of FPGAs
- Back end design of ASICs
**Project Definition**

- The whole DFM paradigm is broken
  - Overly complex rules that are only indirectly related to yield
  - Slow overly complex checkers slowing down custom design
- Solution will improve full custom design productivity and yield

**Progress**

- Initial goal: Demonstrate feasibility on one rule.
- Project split into three after award:
  - DRC with DNN
  - Automated back end flows for ASICs
  - Automated back end flows for FPGAs
  - Made good progress on each

**Results and Significance**

- DRC with DNN sub-project
  - Developed training set based on SRAM class project using NCSU 15 nm PDK
  - Trained TensorFlow tflearn/keras
  - 80% recognition rate on retained data for M1 rule

**Future Outlook**

- Improve recognition rate by increasing orthogonality of training set, and increasing its size
  - And improving network
- Broaden to other rules
- Start structuring yield monitor and layout optimization follow-ons
### Project Definition

- How to set up design in FPGA tools to get predictable design success?
  - Clock
  - FPGA choice
  - Design params
  - Etc.
- Synthesis, P&R time
- Resource Usage
- Slacks
- Etc.

### Results and Significance

- Demonstrated can build accurate and useful models

### Progress

- Initial goal: Demonstrate feasibility on one design.
- Used Surrogate Modeling to build models for Xilinx and Altera FPGAs for specific designs

### Future Outlook

- Demonstrate use of models to set up tools
- Implement classification techniques so that models can be built that will apply to a wide range of designs
Project Definition

- How to set up design in ASIC tools to get predictable design success?
  - Clock Tree
  - Density
  - Design params
  - Timing setup

Future Outlook

- Demonstrate use of models to setup tools in both major vendor’s flows
- Implement classification techniques so that models can be built that will apply to a wide range of designs

Progress

- Initial goal: Demonstrate feasibility on one design.
- Used Surrogate Modeling to build models for back end flow for specific designs for one major EDA vendors tools
- Demonstrated success in improved design convergence

Results and Significance

- Demonstrated can build accurate and useful models
  - Synthesis, P&R time
  - Congestion
  - Slacks
  - DRCs
1A5 Behavioral Model Development for High-Speed Links

Pls: M. Swaminathan, P. Franzon & J. Schutt-Aine
Post Doc: M. Larbi
Students: H. Yu, H. M. Torun, T. Nguyen and B. Li
Year 1 Allocation $166,182
October 12, 2017
Multiple University Project

1. Building models using time domain data and neural networks
   M. Swaminathan, GT

2. Building models using X-parameters and neural networks
   J. Schutt-Ainé, UIUC

3. Building receiver models using system identification and system modeling
   P. Franzon, NCSU
## 1A5 Behavioral Model Development for High-Speed Links (Time Domain)

### Project Definition
- Develop methods that use ML for the automated behavioral modeling of complex circuits that:
  1. Has same accuracy as transistor-level models.
  2. Requires 25X–50X less CPU time & Protects IP.
  3. Is significantly more accurate than IBIS.
  4. Is parameterized, accounts for varying channel conditions and compatible with existing tools
- Relevance to Industry: Accurate models required for system level simulation that protects IP; IBIS models are inaccurate

### Results and Significance
- Enhanced & Augmented Neural Network model developed for fixed frequency oscillators; 10X speed-up (Cadence)
- New behavioral model developed for VCO using augmented + feedforward network; 15X speed-up
- Developing training methodology for I/O circuits for companies that cannot share circuits (Qualcomm);
  Behavioral modeling using RNN in progress
- Developing modeling framework for switching regulators

### Progress
- Milestones:
  - Year 1: Preliminary methods that use ML for the generation of beh. models for circuits used in high-speed signaling. Comparison for accuracy/speed.
  - Year 2: Compatible (w/ commercial tools) automated software for behavioral model and SPICE netlist generation; Tech. transfer
  - Deliverables: Year 1: Beh. models w/ accuracy, speed, and memory for 5–10 ports; Year 2: Software that automates behavioral modeling and SPICE netlist generation (10–20 ports; 25X–50X speed-up)
  - Publications: EPEPS ‘17 (accepted)

### Future Outlook
- Behavioral modeling of transistor circuits that includes methodologies for automated training and model construction using RNN (Qualcomm)
- Behavioral modeling of HSSCDR for generic model construction based on transfer learning using Deep Neural Networks (IBM)
- Behavioral modeling of switching regulator circuits (buck converter); poses unique challenges
Objective and Experimental Plan

- Develop methodologies for automated training for generating behavioral models; Use RNN for generating behavioral models of transistor circuits that are compatible with circuit simulators; Generate Spice netlists
- Apply to examples provided by Qualcomm
- Note: Qualcomm cannot share transistor level circuits but can share simulation data; Qualcomm has provided 4K simulations (mentor: Jaemin Shin & Tim Michalka)
Objectives and Experimental Plan (Time Domain) – cont.

Objective and Experimental Plan
- Develop behavioral models of high speed channels that are generic using Transfer Learning; Apply to HSSCDR from IBM for different topologies (mentor Jose Hejase & Dale Becker)
- Traditional ML uses different models for different but related tasks (separate DNNs for separate topologies)
- Transfer learning can leverage previously trained model and extend it for a related task.
- Overcomes overwhelming process of collecting training data for each task.
Objective and Experimental Plan

- Develop behavioral models of switching regulator circuits (Ex: Buck Converters) that have highly nonlinear behavior and often times are represented using simple matlab models during optimization; Capture both the On/Off modes determined by the switching logic as well as Continuous & Discontinuous mode
- Apply to COTS buck converter (transistor spice netlist available) and Integrated Voltage Regulator that uses 130nm Global Foundries Buck Converter Chip (Georgia Tech)
## 1A5 Behavioral Model Development for High-Speed Links (X-Parameters)

### Project Definition
- Use X-parameters and ML for buffer models
- Relevance to Industry: Alternative to IBIS

### Results and Significance
- X-parameters contain information relevant to IBIS models (X2ibis)
- Volterra kernel (VK) extraction will lead to more accurate simulation
- 2-tiered approach (rational and impulse function approximation)

### Progress
- Milestones: proof of concept established
- Deliverables: Reports
- 1 conference paper delivered, 2 in preparation

### Future Outlook
- Outlook is to offer a neural-based behavioral model extraction module that is pluggable into existing EDA simulation tools
Objectives and Experimental Plan (X-Parameters)

- **Complete 2\textsuperscript{nd} order ANN-aided VK extraction**
  - Using \textit{rational} function approximation
  - Using \textit{impulse} function approximation

- **Implement transient simulation of nonlinear block**
  - Multi-level recursive convolution
  - Point matching delay method

- **Perform benchmark against IBIS method**
  - Simple CMOS inverter
  - Standard I/O Buffer
<table>
<thead>
<tr>
<th>Project Definition</th>
<th>Results and Significance</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Predict a signal accurately at the output of the receiver (RX) based on the input signal.</td>
<td>• Compared linear System Identification models, ARX, ARMAX, State Space; Among linear System Identification models, State Space models show better accuracy.</td>
</tr>
<tr>
<td>• Use system identification to add power-supply-induced jitter into the input signal and build a receiver model.</td>
<td>• Compared State Space model and nonlinear system identification models. Nonlinear models have the best performance.</td>
</tr>
<tr>
<td>• For both simulation and measured systems</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Progress</th>
<th>Future Outlook</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Measured receiver input and output data and use input-output data pair to build different types of system identification models with high accuracy</td>
<td>• Adjoint State-Space Dynamic Neural Network Technique for Nonlinear Modeling.</td>
</tr>
<tr>
<td>• Compared different model performances and select the best one for future use.</td>
<td>• Power supply induced jitter classification.</td>
</tr>
<tr>
<td>• Turned to nonlinear modeling.</td>
<td></td>
</tr>
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</table>
Objectives and Experimental Plan (Receivers)

- Improve model performance using Adjoint State-Space Dynamic Neural Network Technique.
- Determine how to classify PSIJ
- Determine how to model PSIJ
Milestones and Deliverables

- **Time Domain**
  - Software that automates the behavioral model construction and SPICE netlist generation; Application to high-speed SerDes channel with 10–20 ports.
  - Demonstration of 25X–50X speed-up.

- **X-Parameters**
  - 2nd order VK-ANN I/O Buffer modeling module
  - Tailored to fit as a plug-in upon request
  - Assessment of need for higher order

- **Receiver**
  - June, 2018:
    - Complete baseline model
    - Deliver model format and support code
    - Identify PSIJ classification approach
  - December, 2018:
    - Complete PSIJ modeling
    - Deliver model format and support code

- Comparison between methods developed for determining best technique for a class of circuitry.
## Budget Request

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<th>Category</th>
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<th>Cost (per year)</th>
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<td>0 + 15,963 + 18,312</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
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<td><strong>$166,182</strong></td>
</tr>
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Note: We are leveraging from other projects. So, there will be one more GRA working on the problems related to this project (Time Domain).
1A6 Models to Enable System-level Electrostatic Discharge Analysis

PI: Elyse Rosenbaum
Students: Zaichen Chen and Jie Xiong
Year 1 Allocation: $63,746
October 12, 2017
Project Definition

- System-level ESD reliability is achieved through an inefficient process of trial & error
- Simulation has been proposed as a solution
- Roadblock: ESD models of the system components are needed but are not provided
- Solution: Develop a methodology to learn accurate and computationally-efficient ESD models
- Industry impact: Products have shorter time-to-market & greater reliability

Progress

- Milestones: Acquire training data to model components and soft failures (completed); develop techniques to achieve accurate models across the feature space (in progress)
- Deliverables: Multi-port models for ICs (in progress), stochastic models for air discharges (in progress)

Results and Significance

- RNN for transient models of nonlinear circuits
  - A novel regularization term is added to loss function to penalize unstable models
  - Continuous-time Verilog-A implementation of RNN for circuit simulation
- PDN-aware component ESD models
- Chip-board interaction
- Stochastic (“generative”) modeling of air discharge
  - First step toward predictive modeling of soft failures

Future Outlook

- Year one work enables 4 different simulation methodologies (of varying complexity); case studies needed to quantify pros and cons of each
- Generative models will impact system ESD design and test
  - Test conditions and number of tests
  - Design variables (features) vs. failure likelihood
- Demonstrate use of multi-port models to simulate ESD noise coupling at the package and board levels
- Additional applications of RNN circuit models
Objectives and Experimental Plan

- **Benchmark 4 ESD simulation approaches against measurement data**
  - Circuit simulation vs. hybrid EM-circuit simulation
  - I-V model vs. transient model of system components

- **Explore limitations of RNN models / other uses of RNN**
  - Applications other than ESD (e.g., Verilog-AMS behavioral model for mixed-signal simulations)
  - Identify why model provides a very good fit only in most cases & use that information to develop an alternative

- **Finer-grained modeling of package-level ESD current return path**
  - Facilitates simulation of ESD noise coupling (source of soft errors)
  - Challenge: limit the model complexity so it is suitable for hybrid simulator

- **Generative models of ESD and soft failures**
  - Failures are non-deterministic
    - Likelihood = \( f(\text{ESD current pulse, use condition (e.g., instruction being executed, EUT face up or face down, EUT physical construction)}) \)
  - Identify the primary features (generate data from physical experiments)
  - Develop computationally-efficient generative models
    - Currently using kernel density estimation; easy but not efficient
Milestones and Deliverables

Deliverables

1. **Python or MATLAB code. These codes will**
   a. Create an ESD model of an IC’s external pin(s) from data
      - Choice of PDN-aware model or multi-port model
   b. Construct a generative model of air electrostatic discharge parameters
      - $p(I_{\text{peak}}, t_{\text{rise}} | V_{\text{precharge}}, \text{approach speed}, \text{trigger height}, \text{EUT dimensions})$

2. **Report on RNN models of nonlinear circuits with enhanced dynamic range**

Milestones

1. Quantify RNN complexity vs. number of circuit nodes and number of ports
2. Compare simulated ESD waveforms with measurements
3. Demonstrate soft failure prediction capability
4. Implement RNN models in Verilog-AMS and benchmark against other behavioral models
# Budget Request

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Second project PI will be added for year 2, M. Raginsky.
1A7 Optimization of Power Delivery Networks for Maximizing Signal Integrity

PIs: M. Swaminathan & C. Ji
Post Doc: M. Larbi
Students: H. M. Torun & M. Ahadi

Year 1 Allocation $76,500
October 12, 2017
**Project Definition**

- Develop ML based methods to optimize (and model) the output responses of a system given a large set of input (or control) parameters. Examples: High Speed Link, 3D, IVR, WPT for IoT.
- Objective: High dim. problems (>5 params (Year 1); >10 param. (Year 2); 5X-10X improvement in CPU.
- Relevance to Industry: Design optimization is a problem that addresses all systems. Most methods are limited today for high dim. problems.

**Results and Significance**

- Two stage Bayesian Optimization (TSBO)
- 3D Integration: 5 params; 4X faster; Improved skew (12.3%) & temp (9.4%)
- IVR: 5-12 params; 56%-73% faster; Improved eff. (3%-6%) and inductor area (40%)
- WPT: 12 params; 63%-74% faster; Improved eff. (12%), RF (50%-79%) inductor area (28%-61%)
- BER: $10^7$ bit results from $10^5$ bit sim. (preliminary)

**Progress**

- Milestones:
  - Year 1: BO for optimization with 5+ params. Compare with non-ML methods. Apply to two apps.
  - Year 2: BO for optimization with 10+ params. Compare with non-ML methods. Apply to two apps. Tech. transfer to industry.
- Deliverables: Tech. transfer to industry; optimization of systems with 25+ params fully automated.
- Publications: TVLSI ’17 (pub); TVLSI ’17 (under review); Invention Disclosure ’17; EPEPS ‘17 (accepted); Designcon ’18 (accepted); Two ECTC ‘18 (submitted)

**Future Outlook**

- Extend TSBO to 30+ parameters. Apply to systems that include block level interactions. Apply to HSSCDR (IBM); IVR & WPT for IoT.
- Apply to statistical analysis for BER computation. Requires ML based kernel estimation (selection and bandwidth). Develop adapted basis methods to prioritize parameters based on sensitivity. Combine with optimization technique to determine best BER. Apply to HSSCDR (IBM)
- Technology transfer to industry
Objectives and Experimental Plan

- Extend Two Stage Bayesian Optimization to 30+ parameters for global optimization
- Compliment IBM’s HSSCDR tool to identify worst case channel performance to account for manufacturing deficiencies in packages and interconnects (Mentors: Jose Hejase & Dale Becker)
- Apply for the co-optimization of blocks that maximizes performance and minimizes area (Ex: IVR & WPT for IoT)

### Computational Budget for Optimization

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<th>Current Progress</th>
<th>ML Competitor</th>
<th>Non-ML Competitor</th>
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<td><strong>3D IC</strong></td>
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<tr>
<td><strong>IVR</strong></td>
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<tr>
<td><strong>WPT</strong></td>
<td>45-65 Simulations</td>
<td>115-125 Simulations</td>
<td>&gt;250 Simulations</td>
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<td><strong>GOAL</strong></td>
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<td>300-400 Simulations</td>
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<td>(30 Parameters)</td>
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Objectives and Experimental Plan (cont.)

- Ensuring BER of <10⁻¹² for High Speed Links requires prohibitively long CPU time
- Current methods rely on MC based techniques (expensive) or statistical extrapolation (erroneous)
- Objective: Apply ML based methods that predict BER but with reduced simulations (Goal: 100X speed-up)
- Plan is to apply ML for kernel estimation and combine with PC for reduced basis. Adapted basis (Ghanem et al) can then be used to prioritize parameter sensitivity leading to a path towards solving high dimensional problems. Non-linearities included as part of the plan. Goal is to develop a non-intrusive method.

\[
BER(\tau) = P(V_{rx} > 0 | V_{tx} < 0) + P(V_{rx} < 0 | V_{tx} > 0)
\]

\[
BER(\tau) = \int_{0}^{+\infty} PDF_{ab}(\eta) d\eta + \int_{-\infty}^{0} PDF_{cd}(\eta) d\eta
\]

PDF\textsubscript{ab} and PDF\textsubscript{cd} needs to be calculated from a limited set of samples

---

Objective and Experimental Plan

- Ensuring BER of <10⁻¹² for High Speed Links requires prohibitively long CPU time
- Current methods rely on MC based techniques (expensive) or statistical extrapolation (erroneous)
- Objective: Apply ML based methods that predict BER but with reduced simulations (Goal: 100X speed-up)
- Plan is to apply ML for kernel estimation and combine with PC for reduced basis. Adapted basis (Ghanem et al) can then be used to prioritize parameter sensitivity leading to a path towards solving high dimensional problems. Non-linearities included as part of the plan. Goal is to develop a non-intrusive method.
Milestones and Deliverables

- ML based BO that supports 30+ parameters. Apply to HSSCDR, IVR & WPT for IoT.
- Develop ML based kernel estimation methods for BER estimation for high speed links. Develop adapted basis for addressing parameter sensitivity for high dimensional problems.
- Compare with non-ML and other ML methods
- Develop Software (in Matlab) for implementing ML based BO and BER estimation that is automated (NO manual intervention)
- Technology transfer to industry
# Budget Request

## Category

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<td>$18312</td>
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<tr>
<td>TOTAL</td>
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<td>$76,500</td>
</tr>
</tbody>
</table>

Note: We are leveraging from other projects. So, there will be one more GRA working on the problems related to this project.
Lunch & Poster Session
Next Door

IAB resume here 2:00 pm to complete LIFE forms

All others return at 2:15 pm
http://iucrc.com

Password: CAEMLFall2017
New Project Proposals

30 minutes each:
- 20 minute presentation, 5 minute Q&A,
- 5 minute LIFE form completion

2:15 – 4:15
2A1 Security-centric synthesis and optimization for trusted hardware design

Deming Chen, Illinois
October 12, 2017
Project Problem Statement

• **What problems do we solve?**
  - Security and trust concerns of SoCs (System-on-a-Chip)
  - Hardware becomes too expensive after brute-force security features are added

• **Relevance to industry**
  - While cybersecurity has been an heavily studied topic in the research community, the assumption is that the hardware systems are secure themselves
  - However, security and trust in integrated circuits themselves remain an ongoing concern
    - A security breach at the hardware-level exposes even provably secure algorithms and protocols to vulnerabilities
  - This project focuses on SoC hardware security
    - Improve it while saving additional cost
    - Very relevant to industrial goals
Long-term Vision and Goals

• Novel security-centric synthesis and optimization techniques for secure and trusted hardware system design.

• A new design methodology, where the SoC hardware is designed through hardware/software co-design, high-level synthesis (HLS), and machine learning (ML) for security.
Project Objectives

• Demonstrate that there is an effective trade-off among security, power consumption, and area cost for hardware systems design, and our machine learning method is able to identify the best such trade-offs given resource/cost constraints.

• Demonstrate that proposed new architecture and synthesis techniques are able to significantly improve hardware system security without incurring high resource overhead.

• Demonstrate that our machine learning techniques can identify malicious attacks and come up with countermeasures effectively.
Threat Model in Hardware Security

- Trojan injection
- Side-channel information leakage
- Logic attack
- Eavesdropping
- Intrusion and fault injection
- Security vulnerability of embedded software
- Counterfeit / Reverse Engineering / IP Piracy
- ...

...
Security Centric Hardware Design

- Essential tradeoff of security centric hardware design

  Security features
  - Hardware redundancy
  - Dispersed cipher paths
  - ...

  Hardware cost
  - Power & Energy
  - Resource
  - Performance

  How to find the optimal balance?

- Automatic hardware/software co-design framework

  Application C/C++ ➔ System Partitioning Engine ➔ Performance ➔ Power ➔ Security level

go.illinois.edu/caeml
Hardware-Software Co-Design Framework for Security

New features to extend to security centric hardware design:

- Critical region identification
- Security modeling for both software and hardware
- Annotation with security metrics
- Refined ILP solver
- Refined system evaluation scheme

[ICCAD’15 (best paper award), ICCAD’16, DAC’17]
• **Drawback of ILP based solution: Scalability**
  - Hardware-Software partitioning is a *classification problem*
  - It is possible to apply machine learning for large designs

• **ML hardware-software partitioning framework**

![Diagram of ML based Hardware-Software Partitioning](diagram.png)
Novel Architecture Optimizations

- Information dispersion through replication of execution paths
  - Cipher key separated into sub-segments and distributed among replicated paths for not exposing a single point of vulnerability
  - Determine the right information dispersion

- Control flow obfuscation
  - Dynamically change the control flow while maintaining functionality
New HLS for Security

- New scheduling, resource allocation, and binding algorithms during HLS (high-level synthesis)

- Smart operations and data mapping onto target architectures to protect against attacks

- Evaluate results with simulation and FPGA emulation

Work with different strategies for timing attacks; power attacks; or EM attacks
• In cybersecurity, various learning techniques have been proposed to identify attacks
  o When datasets are available: supervised learning
  o Otherwise: unsupervised learning

• Dynamic analysis (detection at runtime)
  o Heuristic analysis from the underlying action/execution
  o No need for source code, but may not cover all the execution paths

• Static analysis (detection at source-code level)
  o Full view of the program but usually require source files
  o Need to differentiate good from bad

• Question: would similar or enhanced machine-learning techniques applicable to hardware system security?
ML in Hardware Security

• Machine learning to classify and evaluate threats
  o Use of novel ML techniques (e.g. bidirectional LSTM to capture global patterns or attack sequences)
  o Use normal profiles for training on different machine learning models
  o What are the best models for identifying sophisticated scenarios and mixed attacking strategies?

• Countermeasure in design
  o Testing and verification against various attacks
    ▪ Use SoC FPGAs
  o Self-protection
    ▪ Such as entering protected safe-mode after being compromised
  o Obfuscation of real information
<table>
<thead>
<tr>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jan 1, 2018</td>
<td>Project Start</td>
</tr>
<tr>
<td>Sep 1, 2018</td>
<td>Comprehensive Pareto Curve for designers to make the right decision for highly secure hardware design under resource constraints.</td>
</tr>
<tr>
<td>May 1, 2019</td>
<td>New architecture-level optimization and synthesis techniques to improve security of hardware systems.</td>
</tr>
<tr>
<td>Jan 1, 2010</td>
<td>Novel machine learning techniques to evaluate, identify, and assess different and sophisticated attacking strategies/scenarios and come up with counter-mechanism against such attacks.</td>
</tr>
</tbody>
</table>
Deliverables and Outcomes

• **Year 1:**
  - Presentation and publication to validate the proposed ideas focusing on design space exploration with machine learning and initial solutions for new secure architecture design and synthesis method.

• **Year 2:**
  - Presentation and publication to validate the proposed ideas focusing on advanced architecture design and synthesis for security and machine learning techniques to identify malicious attack quickly and provide countermeasure.
Collaborators and Resources

• **Resources**
  - Our open source hardware/software co-design package
  - Our high-level synthesis works on hardware security
## Proposed Budget

<table>
<thead>
<tr>
<th>Category</th>
<th>Number</th>
<th>Cost (per year)</th>
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<td><strong>TOTAL</strong></td>
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2A2 Machine Learning for Trusted Platform Design

New Project Proposal

A. Raychowdhury & M. Swaminathan, GaTech
October 12, 2017
Problem Statement: Trusted IoT Platforms and Security Vulnerabilities

Security vulnerabilities of IoT nodes include:

1. **Power side channel attack** during AES encryption
2. **EM side channel attack** via near and far fields
3. **RF channel attack**

Relevance to Industry: Methodologies and designs developed as a part of this project will open up opportunities for trusted electronics.
Proposed Solution

- We will train an adversarial network for both reactive and proactive side channel attacks.
- Adversarial networks will be able to detect potential attacks within ms.
- Embedded sensors will provide data for training and analysis.
Project Objectives

We will demonstrate:
1. Adversarial networks (proactive and reactive) that act as embedded observers in IoT nodes.
2. Capability of detecting attacks (RF, power or EM side channel) within milliseconds.
3. Low overhead (<10%) circuit topologies and architectures to detect side channel attacks.
We will demonstrate:

1. Year 1: Model based adversarial networks and capability for detecting attacks
2. Year 2: We will use COTS test boards to evaluate the solutions developed. If possible, we will use a custom designed and fabricated board at GT that supports Wireless Power Transfer for IoT.
ANN based observer can be used to monitor system states and allows us to use the model predictive and state estimation theory that has been developed in the observer based control design.

Use of ANN in the observer state (model-free observer) will help open up key opportunities to design robust and secure power delivery networks.
## Annual Milestones

<table>
<thead>
<tr>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Date: Jan 1, 2018</td>
<td>Project Start</td>
</tr>
<tr>
<td>Date: June 1, 2018</td>
<td>Develop ML methods based on both diagnostic and active learning techniques using ANN and Bayesian Inference methods.</td>
</tr>
<tr>
<td>Date: Nov 1, 2018</td>
<td>Apply Deep Learning techniques for detecting minute changes in the system response in milli-seconds.</td>
</tr>
<tr>
<td>Date: Dec 31, 2018</td>
<td>Develop a proof of concept strategy that can be used to extend the solution and its verification in Year 2.</td>
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</table>
# Deliverables and Outcomes

<table>
<thead>
<tr>
<th>Year 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Models of the system that include RF communication, WPT and security blocks that includes near field coupling through RF coils at ~1GHz using HFSS, ADS and Matlab</td>
</tr>
<tr>
<td>2. Model of adversarial network as an observer</td>
</tr>
<tr>
<td>3. Algorithms developed in Matlab for deep learning based on ANN and Bayesian Inference methods</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Year 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Model based demonstration of counter measures</td>
</tr>
<tr>
<td>2. Prototype development with observer</td>
</tr>
<tr>
<td>3. Demonstration of trusted platform using prototype or evaluation board</td>
</tr>
<tr>
<td>4. Software for Deep Learning in matlab</td>
</tr>
</tbody>
</table>
Collaborators and Resources

• **Collaborator**
  - Chuanyi Ji, GT

• **Equipment and previous work to be leveraged**
  - In Year 1 our focus will be on modeling only. We will define the IoT system and develop deep learning models, the adversarial networks (observers) and attacks all in a matlab environment.
  - In Year 2 our focus will be on refining these models and testing them on an evaluation board as well as look into the WPT board for IoT being developed at GT.
  - We will leverage from several years of experience (design, modeling, fabrication and verification) in the areas of RF, power delivery, EM and ANN to develop unique solutions
## Proposed Budget

<table>
<thead>
<tr>
<th>Category</th>
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<td>Tuition waivers</td>
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<td><strong>TOTAL</strong></td>
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<td><strong>53,345</strong></td>
</tr>
</tbody>
</table>

Note: We are leveraging from other projects. So, there will be one more GRA working on the problems related to this project.
2A3 Causal Inferencing for Building Trust in Platform Designs

New Project Proposal

S. Vasudevan
October 12, 2017
Trusted platforms

• **Platform attacks have increased manifold**
  - Overseas manufacturing, IP reuse, Long supply chains, programmable devices...

• **Urgent societal problem**

• **Solution**
  - Long term
  - Constraints of cost and performance
  - Effective in detecting and protecting threats
Proposed Solution: Lifelong trust

- Automate threat analysis in the hardware design
- Improve efficiency and coverage of complex system analysis
- Analyze data during operation for compromises
- Update detection and analysis based on continuous monitoring during operational lifetime
Project Objectives

- Develop methodology for low cost, high performance threat analysis in platform systems
- Investigate the efficacy of cross layer threat detection between software and hardware layers
- Develop methods to provide feedback to efficient machine learning algorithms to incorporate lifelong trust
GoldMine: Integrating solution spaces

Execution Traces

Domain Information
Static Analysis

"Interesting" System Behavior

Statistical Techniques
Machine learning

Hardware
Software
Embedded Systems

Dynamic System Data
Relevant Knowledge

Combine both to offset their disadvantages
Cross layer causality inferencing

- False positives occur due to alerts that are correlated, but not causal
- Hardware checkers costly; software checkers slow
- Causal inferencing is difficult for statistical (machine learning) methods
- **GoldMine**
  - Systematically analyzes the domain
  - Interfaces with machine learning algorithms
  - Causality inferencing
GoldMine flow

**ASSERTIONS**

- Temporal Assertions
- System Invariants
- Counter-examples
- Feedback

1. **Design**
2. **Static Analysis** (Design Constraints)
3. **Data Generator** (Simulation Traces)
4. **A-Miner**
5. **Formal Verification**
6. **A-Val**
Automate threat analysis in design

- **Cross layer assertion-based analysis**
- **Hardware assertions using GoldMine**
  - Assertions ranked according to coverage, importance and succinctness
  - Top assertions selected for synthesis in hardware
  - Critical system level hardware properties
- **Software level assertions**
  - Generated from typical workload application software with machine learning algorithms
- **When something is violated…**
  - Analyze application level and hardware assertions jointly for reducing false positives
Diagnosing a violation

• Coverage analysis tool in GoldMine
  o Identifies parts of the design covered by an assertion
  o Scalable computation in a very large space

• Violation of a GoldMine assertion
  o Find the unexpected behavioral pattern
  o Map it back to design
  o Identify possible culprit hardware IP that was tampered

• Transaction level coverage
  o Zooming in on culprit transactions from running application
  o Concurrent episode mining
  o Scalability: big challenge
  o Post-Silicon debug methods for OpenSparc T2 SoC
Online and lifetime analysis

- Software detectors are adaptable
- Online data collection and feedback
  - New applications and transactions constitute “new data”
  - Application level assertions updated periodically
  - False positives, false negatives and undetected tampering cases recorded
- Machine learning algorithms for software assertion generation
  - Transaction and application level data
  - Feedback from “holes” like false positives, false negatives etc.
  - Converge very quickly to excellent assertions
  - PRISM, RIPPER, Metapath analysis: Enhance with feedback
## Annual Milestones

<table>
<thead>
<tr>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jan 1, 2018</td>
<td>Project Start</td>
</tr>
<tr>
<td>May 10, 2018</td>
<td>Application level assertion generation</td>
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<tr>
<td>August 10, 2018</td>
<td>Joint analysis engine for cross layer detection</td>
</tr>
<tr>
<td>December 10, 2018</td>
<td>Experimental validation by attack injection on OpenSparc T2</td>
</tr>
</tbody>
</table>
Deliverables and Outcomes

• **First year**
  o Algorithms for partitioning design behavior into hardware level detectors and software detectors
  o Algorithms for generating application level assertions for tamper detection
  o Prototype software working on experimental testbed (OpenSparc T2)

• **Second year**
  o Algorithms for coverage analysis at transaction level for diagnosis
  o Methods for online data collection and feedback
  o Algorithms to make machine learning algorithms “learn” tampering behavior and predict tampering
## Proposed Budget

<table>
<thead>
<tr>
<th>Category</th>
<th>Number</th>
<th>Cost (per year)</th>
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<td>Grad. students</td>
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<td>Indirect costs</td>
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<td><strong>50,000</strong></td>
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</table>
2A4 Machine Learning to Predict Successful FPGA Compilation Strategy

New Project Proposal

Sung Kyu Lim, GaTech
October 12, 2017
Goal
- Build ML models that produce FPGA compilation recipes
- Objectives: high success rate and fast compilation time

Industry relevance
- FPGAs are hugely popular for machine learning
- Compilation today: trial-and-error with human intervention
- Compilation tomorrow: ML-based with no human intervention
Proposed Solution

• **Input to us**
  - RTL with timing constraint
  - Target FPGA device
  - FPGA compilation toolset
    - synthesizer, mapper, placer, router
  - Compilation *recipe*
    - optimization goal: performance vs. power
    - optimization effort level: low, medium, high
    - algorithmic parameters

• **Our ML model predicts**
  - If the RTL will fit in the FPGA using the current recipe
  - If the timing constraint is met
  - How long the compilation will take
  - Best one if multiple recipes are given
• **We will demonstrate that ML is capable of**
  - Predicting FPGA compilation success
  - Predicting FPGA compilation time
  - Evaluating a given compilation recipe
  - Rank-ordering multiple recipes

• **We will investigate how to**
  - Extract *key compilation parameters*
  - Learn how they co-relate
  - Train ML models
  - Influence compilation toolset algorithms
Approach: ML Model

• **Our big data**
  o Existing FPGA compilation database
  o Both successful and unsuccessful

• **ML model inputs**
  o Design parameters
    ▪ # of LUTs, FFs, global signals, I/Os
    ▪ netsize distribution
  o Toolset parameters
    ▪ optimization goals/efforts
    ▪ algorithmic parameters

• **ML outputs**
  o Compilation success rate and time
  o Local congestion
Improving Local Congestion

• During synthesis
  o Minimize # of nets and pins

• During mapping
  o Minimize # of connections among logic elements

• During placement
  o Minimize wirelength while avoiding congested spots

• During routing
  o Avoid local hotspots while minimizing detours

• But these tricks may worsen compilation time
  o Strike a balance between congestion vs. compilation time
Targeting Multi-FPGA Systems

- **Silicon interposer**
  - Key technology today to integrate multiple FPGAs onto a single chip

- **FPGA partitioning** becomes a key step
  - Determines # of I/Os
  - Determines # of interposer interconnects
  - Ultimately affects multi-FPGA compilation success and runtime
Multi-FPGA Partitioning

- **Challenges**
  - Imposing *pin constraint* is hard
  - Imposing *interposer interconnect limit* is hard

- **How can ML help?**
  - Find compilation *recipes* that improve FPGA partitioning quality
  - May propose new/improved partitioning schemes
Annual Milestones

<table>
<thead>
<tr>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1</td>
<td>Study the database and extract key parameters that affect success rate, runtime, and congestion for <strong>single</strong> FPGA system</td>
</tr>
<tr>
<td>Q2</td>
<td>Build the initial ML model and train it for <strong>single</strong> FPGA system</td>
</tr>
<tr>
<td>Q3</td>
<td>Deploy the model for prediction and conduct error analysis for <strong>single</strong> FPGA system</td>
</tr>
<tr>
<td>Q4</td>
<td>Extension to <strong>multi</strong>-FPGA system applications</td>
</tr>
</tbody>
</table>
Deliverables and Outcomes

• **Year 1**
  - ML models for single FPGA system
  - Initial ML models for multi-FPGA systems

• **Year 2**
  - Optimized models for multi-FPGA systems
  - Compilation parameter/algorithm enhancements for improved success, runtime, congestion
Collaborators and Resources

• CAEML collaborator
  o Prof. Madhavan Swaminathan (GT)
  o Synopsys
  o Open for suggestion

• Special equipment needed
  o None

• Previous work to be leveraged
  o Knowhow on FPGA place/route (from Aplus Design Technologies)
## Proposed Budget

<table>
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<tr>
<th>Category</th>
<th>Number</th>
<th>Cost (per year)</th>
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LIFE Form Discussion on the five Renewal Proposals from the morning session

Led by D. Becker & D. Hoffman, Attendance restricted to Site Directors, NSF & IAB
Proposals Poster Session
next door
All project proposals; renewal, new and follow-on
4:45 pm – 6:00 pm
Cocktails & Dinner - 6:30 pm
Dorothy and Roy Park Alumni Center

We gather tomorrow morning in Engineering Building II room 3002. Enter the door closest to the West Oval Parking Deck and follow the signs.

Breakfast will be available starting at 7:15
CAEML Center
Semi-Annual Meeting
WELCOME
Day Two – Friday, October 13
2A5 Applying Machine Learning to FPGA Design

New Project Proposal

R. Davis, P. Franzon, D. Baron, NCSU
October 12, 2017
Project Problem Statement

- Back end FPGA SP&R tools have many “knobs” to set
- Relationship of settings to outcomes is not clear, slowing down design

- Industry relevance: Cost of design is high, schedules uncertain
Proposed Solution

• Use Machine-Learning techniques to make sense of complex relationships
• Train computer models that can “fetch” the right knob settings
• Back-end designers become trainers, rather than the knob-turners
Project Objectives

• Demonstrate an FPGA Back-End design flow model that
  o predicts design-flow outcomes from tool settings & RTL with reasonable accuracy
    ▪ Synthesis and P&R time
    ▪ Slacks
    ▪ Resources Utilization
  o reduces design iterations needed to achieve a desired outcome
  o can be generalized to many designs
  o gradually improves as more training data comes available
Model Training Flow

• Uses the same approach that a human designer uses
• Challenges
  o Limited training data
  o Changing flows, gaps in data
• Key Questions
  o Which outcomes/stats matter?
  o How much accuracy is needed?
Proof of Concept in IC Design

- This project proposes a similar approach to the one pursued with IC Design Tools, applied to FPGA tools

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<th>Iter</th>
<th>CLKper</th>
<th>Den.</th>
<th>Lyr</th>
<th>Max Skew</th>
<th>Sink Max Tran</th>
<th>Cong.</th>
<th>Viol</th>
<th>Hold slack</th>
<th>Setup Slack</th>
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<td>400</td>
<td>0.28H/1.51V</td>
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- Surrogate model provides guidance for design & optimization
- Able to achieve an optimal design with 4 iterations
- Human designer took 20 iterations
• Related work shows feasibility [Grewal, IPDPS 2017]
  o Selection of best placement tool for a design, routing prediction
  o This work targets commercial tools, meeting design goals

• Possible Classification Vectors
  o Special resource usage
  o net/gate, net/flop, and net/_adder ratios by region
  o distribution of fan-in & fan-out
**Benchmark/Training Designs**

- **SparseNN SIMD-ASIP**
  - 250 MHz, 29.5 mm², 2.1 W in 65nm CMOS

- **AnyCore OoO Processor**
  - 125 MHz, 25 mm², 40 mW in 130 nm CMOS

- **Others**
  - ISPD Benchmarks?
  - Member-Company-supplied benchmarks?
• (Paritosh Dande) Demonstrated surrogate model for an Altera flow that predicts resource usage on Cortex-M0 design with one setting (clock-period), also explored utilization as a setting.

• (Billy Huggins) Demonstrated a surrogate model for a Xilinx flow that predicts placement outcomes from synthesis outcomes on SIMD pipeline design with speed-grade & directive settings
  o Exhaustive simulation of options for Synthesis, Logic Optimization, & Placement alone yields 1064 possibilities & consumes 100 GB for one speed-grade
  o Including all options up to Route would be 76K possibilities & 7.6 TB of storage
## Annual Milestones

<table>
<thead>
<tr>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jan 1</td>
<td>Project Start</td>
</tr>
<tr>
<td>Apr 30</td>
<td>Basic Model Fit for one design</td>
</tr>
<tr>
<td>Jun 30</td>
<td>Fit Model for all</td>
</tr>
</tbody>
</table>
| Sept 30 | Analysis of Classification Criteria  
           Demonstration of Productivity Gain on One Design |
Deliverables and Outcomes

- **Year 1**
  - (Outcome) Demonstrated viability of model for a specific design/design-goal and impact on design iterations
  - (Outcome) Understanding of how to classify designs
  - (Deliverables) Reports on outcomes and Distribution of Model training data/code on request

- **Year 2**
  - (Outcome) Demonstrated viability of model to achieve specific design-goal without additional model training
Collaborators and Resources

- **Collaborators:**
  - Maxim Raginsky (UIUC) (Informal)

- **No special resources required**
# Proposed Budget

<table>
<thead>
<tr>
<th>Category</th>
<th>Number</th>
<th>Cost (per year)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grad. students</td>
<td>12 months</td>
<td>$26,000</td>
</tr>
<tr>
<td>Faculty support</td>
<td>0.5 months</td>
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</tr>
<tr>
<td>Benefits</td>
<td></td>
<td>$6,600</td>
</tr>
<tr>
<td>Travel</td>
<td>3 trips</td>
<td>$5,000</td>
</tr>
<tr>
<td>Indirect costs</td>
<td>10% rate</td>
<td>$4160</td>
</tr>
<tr>
<td>Tuition waivers</td>
<td># of GRAs</td>
<td>$17,559</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td><strong>53,926</strong></td>
</tr>
</tbody>
</table>
Components in an electrical or electromechanical system wear out and fail

Usual countermeasures

1. Hardware redundancy
2. Hardware retirement prior to projected end-of-life

*These incur a cost penalty, and do not entirely eliminate system-level failures!*

Relevance to industry: CAEML members use (and develop) large-scale arrays of like components

- Storage arrays, computer clusters …
Proposed Solution

• Utilize field sensor data to identify impending failure of a component
• Failure notification must be given *sufficiently far in advance*
  o Such that a replacement can be effected before system performance is compromised
• Realize this solution by utilizing *causal inference*
• Demonstrate approach in the context of HDD failure prediction using S.M.A.R.T. data
• Apply predictor to previously unencountered HDD by using causal transfer learning
SMART Data Analytics

Examples of SMART attributes (~80 total)

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMART 1</td>
<td>Read Error Rate</td>
</tr>
<tr>
<td>SMART 3</td>
<td>Spin-Up Time</td>
</tr>
<tr>
<td>SMART 5</td>
<td>Reallocated Sectors Count</td>
</tr>
<tr>
<td>SMART 9</td>
<td>Power-On Hours</td>
</tr>
<tr>
<td>SMART 194</td>
<td>Temperature</td>
</tr>
<tr>
<td>SMART 204</td>
<td>Soft ECC Correction</td>
</tr>
</tbody>
</table>

- Observed correlation between Annual Failure Rate and Read Error Rates
  - Read Error Rate = 0: Low failure rate
  - Read Error Rate > 0: High failure rate
- Patterns in SMART Data (e.g. Read Error Rate) may be useful for prediction
Project Objectives

• Using SMART time series data, formulate information theoretic bounds on the prediction capability
  o How far in advance can a failure be predicted, irrespective of the algorithm and model

• Advance the state-of-the-art in causal transfer learning

• Evaluate whether causal inference outperforms previously tried methods to construct HDD failure predictors
  o E.g., support vector machines, recurrent neural networks, regression trees
Approach

- Utilize causal inference to discover information in time series data
- **Curse of dimensionality:** data centers collect tens of SMART attributes
  - Causal inference omits redundant covariates or features that might be correlated with the failure but do not help in the prediction task.
- **Model agnostic:** causal inference does not specify what model class should be used to form the failure predictor.
  - User can find an optimum balance between model complexity and achieving the theoretical prediction limit
Approach, cont.

- **Goal:** to find casual influence structure, i.e., graphical model learning
- **Graph:**
  - nodes: random processes
  - directed edges: direction of causal influence
- **Observations:** all (or a subset) of time series of the realizations of processes

- Intimately related to time series analysis
- Econometrics and computational finance
- Financial networks:
  - risk of banking and insurance systems to determine impact of sovereign risk
  - influence structure of stock markets: inter- or intra-market
Granger Causality

Clive Granger (1969):
“We say that X is causing Y if we are better able to predict [the future of ] Y using all available information than if the information apart from [the past of] X had been used.”

- **Granger’s Formulation: AR Model**

\[
Y_t = \sum_{\tau > 0} a_\tau Y_{t-\tau} + b_\tau X_{t-\tau} + c_\tau Z_{t-\tau} + E_t
\]

\[
\hat{Y}_t = \sum_{\tau > 0} \hat{a}_\tau Y_{t-\tau} + \hat{c}_\tau Z_{t-\tau} + \hat{E}_t.
\]

If \( \text{var}(E_t) = \text{var}(\hat{E}_t) \), \( X \not\rightarrow Y \).  

\[
G_{X \rightarrow Y} = \log \frac{\text{var}(\hat{E})}{\text{var}(E)}
\]

- **Past of X does not help prediction.**
Revisiting Granger’s viewpoint

1. Sequential predictors: 
   \[ b_i = g_i(y_i^{i-1}, x_i) \quad \tilde{b}_i = \tilde{g}_i(y_i^{i-1}) \]

2. Outcome \( y \) is revealed, the loss incurred: 
   \[ l(y, b) \]

3. Reduction in loss (regret): 
   \[ \frac{1}{n} \sum_{i=1}^{n} l(y_i, \tilde{b}_i) - l(y_i, b_i) \]

Case:

1. Logarithmic loss: 
   \[ l(y, b) = - \log b(y) \]

2. Predictor: beliefs, then optimal predictors: conditional densities

3. Expected regret is **directed information**: 
   \[ \frac{1}{n} I(X^n \rightarrow Y^n) \]
   \[ \frac{1}{n} \mathbb{E} \left[ \sum_{i=1}^{n} l(Y_i, \tilde{B}_i) - l(Y_i, B_i) \right] = \frac{1}{n} \mathbb{E} \left[ \sum_{i=1}^{n} \log \frac{P(Y_i | X_i, Y_{i-1})}{P(Y_i | Y_{i-1})} \right] \]

   - Non-negative; zero iff future of \( Y \) is independent of past & present \( X \) given past of \( Y \)
   - Applicable to any modality, e.g. point process
There is an arrow from $x_1$ to $x_2$ if

$$I(x_1 \rightarrow x_2 || x_{-\{1,2\}}) > 0$$

$$\{1, 2\} := \{1, 2, \ldots, m\} \setminus \{1, 2\}$$

Resulting graph is a directed information graph.
Neuroscience Application:

- Primate hand movement experiment
- Simultaneously recorded brain cells in motor control region
- Many edges along upward-right diagonal / direction of information propagation in this brain region

Approach

• We have applied our framework for learning in online social networks (such as Twitter data) and analyzing stock market

• Recall:

There is an arrow from $x_1$ to $x_2$ if

$$I(x_1 \rightarrow x_2 || x_{\neg\{1,2\}}) > 0$$

$\neg\{1,2\} := \{1, 2, \ldots, m\} \setminus \{1, 2\}$

• Requires learning a high-dimensional joint probability distribution.
• We propose to use side information about the model class to reduce the complexity of the learning task.
# Annual Milestones

<table>
<thead>
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<tbody>
<tr>
<td>1/1/18</td>
<td>Project Start</td>
</tr>
</tbody>
</table>
| 5/1/18  | Use domain-specific knowledge to develop statistical models for causal inference  
|         | - nonparametric (e.g., intensity functions for point processes)             |
|         | - parametric (e.g., autoregressive models with fixed order)                  |
| 8/1/18  | Identify dataset requirements for parametric and nonparametric approaches   |
Deliverables and Outcomes

• Basic demo of a software implementation
  o Learning parametric or nonparametric point process models from training data
  o Estimating directed informations and building a DIG
  o Eliminating features based on estimated causal influence

• Theoretical analysis of causal inference algorithm complexity and performance
  o Comparison of sample/time complexity for nonparametric vs. parametric approaches.
  o Comparison with fundamental information-theoretic lower bounds

• Technical report summarizing results

• If causal inference is demonstrated to outperform previous methods of failure prediction, a follow-up project proposal will be presented at the end of the year
Collaborators and Resources

- Project will utilize theory and algorithms for causal inference in networks of point processes (already) developed by N. Kiyavash and her group
## Proposed Budget

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<th>Number</th>
<th>Cost (per year)</th>
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</thead>
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<td>Grad. students</td>
<td>1 (9 months)</td>
<td>20,718</td>
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<tr>
<td>Faculty support</td>
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<tr>
<td>Supplies</td>
<td></td>
<td>1000</td>
</tr>
<tr>
<td>Travel</td>
<td>4 trips</td>
<td>4325</td>
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<tr>
<td>Indirect costs</td>
<td>10% rate</td>
<td>2604</td>
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<tr>
<td>Tuition waivers</td>
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<td>12,349</td>
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<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td><strong>$40,996</strong></td>
</tr>
</tbody>
</table>
2A7 Applying Machine Learning to Back End IC Design

New Project Proposal

R. Davis, P. Franzon, D. Baron, NCSU

October 12, 2017
Back end ASIC/SoC Physical-Design tools have many “knobs” to set. Relationship of settings to outcomes is not clear, slowing down design. Industry relevance: Cost of design is high, schedules uncertain.
Proposed Solution

• Use Machine-Learning techniques to make sense of complex relationships
• Train computer models that can “fetch” the right knob settings
• Back-end designers become trainers, rather than the knob-turners
Project Objectives

- Demonstrate an Back-End/Physical design flow model that
  - predicts design-flow outcomes from tool settings & RTL with reasonable accuracy
  - reduces design iterations needed to achieve a desired outcome
  - can be generalized to many designs
  - gradually improves as more training data comes available
Model Training Flow

- Uses the same approach that a human designer uses
- Challenges
  - Limited training data
  - Changing flows, gaps in data
- Key Questions
  - Which outcomes/stats matter?
  - How much accuracy is needed?
# Proof of Concept

## Surrogate model provides guidance for design & optimization

- Able to achieve an optimal design with 4 iterations
- Human designer took 20 iterations

<table>
<thead>
<tr>
<th>Iter</th>
<th>CLKper</th>
<th>Den.</th>
<th>Lyr</th>
<th>Max Skew</th>
<th>Sink Max Tran</th>
<th>Cong.</th>
<th>Viol</th>
<th>Hold slack</th>
<th>Setup Slack</th>
<th>Comments</th>
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<tbody>
<tr>
<td>1</td>
<td>10</td>
<td>0.6</td>
<td>8</td>
<td>300</td>
<td>400</td>
<td>0.28H/1.51V</td>
<td>105</td>
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<td>6.46ns</td>
<td>Over-congested; Hold time violated</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>0.5</td>
<td>8</td>
<td>300</td>
<td>400</td>
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<td>6.55ns</td>
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</tr>
<tr>
<td>3</td>
<td>10</td>
<td>0.45</td>
<td>8</td>
<td>300</td>
<td>400</td>
<td>0.02H/0.11V</td>
<td>0</td>
<td>2.4ps</td>
<td>6.48ns</td>
<td>No DRC errors; hold fixed; hold margin is low</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>0.45</td>
<td>8</td>
<td>200</td>
<td>300</td>
<td>0.02H/0.17V</td>
<td>0</td>
<td>10.5ps</td>
<td>6.37ns</td>
<td>Final Design</td>
</tr>
</tbody>
</table>

- # of Standard Cells | 39990
- Area ($\mu m^2$)
  - Core: 98109.284 (313.224*313.224)
  - Chip: 54363.008 (233.158*233.158)
- Cell Density: 55.4 %
• **Related work shows feasibility [Grewal, IPDPS 2017]**
  o Selection of best placement tool for a design, routing prediction
  o This work targets commercial tools, meeting design goals

• **Possible Classification Vectors**
  o Special resource usage
  o net/gate, net/flop, and net/adder ratios by region
  o distribution of fan-in & fan-out
Benchmark/Training Designs

- **SparseNN SIMD-ASIP**
  - 250 MHz, 29.5 mm\(^2\), 2.1 W in 65nm CMOS

- **AnyCore OoO Processor**
  - 125 MHz, 25 mm\(^2\), 40 mW in 130 nm CMOS

- **Others**
  - ARM Cortex-M0 SoC (0.1 mm\(^2\) in 45nm CMOS)
  - ISPD Benchmarks
  - Member-Company-supplied benchmarks?
  - Will likely be re-worked for 32nm and/or 14nm technology
Progress to Date

- Anngenetic model for global-route outcomes
- Linear regression model for power and area
- Neural Networks model for hold slack
- Decision Tree models for the number of DRC violations
### Surrogate GR Modeling Results

<table>
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<tr>
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<th>area_trial</th>
<th>TNS</th>
<th>violating_path</th>
<th>WNS</th>
<th>x_neg_1_4</th>
<th>x_neg_5_8</th>
<th>x_pos_0_10</th>
<th>x_pos_11_20</th>
<th>hold_slack_trial</th>
<th>power_trial</th>
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<td>0.181</td>
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<td>0.473</td>
<td>0.441</td>
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<td>0.966</td>
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<td>0.798</td>
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<td>0.812</td>
<td>0.791</td>
<td>0.808</td>
<td>0.829</td>
<td>1.064</td>
<td>1.397</td>
</tr>
</tbody>
</table>

The Root Relative Squared Error (RRSE) is relative to squared error compared to a simple predictor (the average of values).

\[
RRSE = \sqrt{RSE} = \sqrt{\frac{\sum (f(x_i) - y_i)^2}{\sum (\bar{y}_i - y_i)^2}}
\]

RRSE is close to 0 → model is much better than a simple predictor
RRSE is close to or larger than 1 → model is worse than a simple predictor
RRSE < 0.5 is the target.
# Annual Milestones

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<td>Fit Model for one design including Power-Rail &amp; Clock-Tree Insertion</td>
</tr>
<tr>
<td>Sep 30</td>
<td>Fit Models for all benchmark circuits</td>
</tr>
<tr>
<td>Dec 31</td>
<td>Analysis of Classification Criteria Demonstration of Productivity Gain on One Design</td>
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Deliverables and Outcomes

• Year 1
  o (Outcome) Demonstrated viability of model for a specific design/design-goal and impact on design iterations
  o (Outcome) Understanding of how to classify designs
  o (Deliverables) Reports on outcomes and Distribution of Model training data/code on request

• Year 2
  o (Outcome) Demonstrated viability of model to achieve specific design-goal without additional model training
Collaborators and Resources

- **Collaborators:**
  - Maxim Raginsky (UIUC) (Informal)

- No special resources required
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<tr>
<td><strong>TOTAL</strong></td>
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<td><strong>53,926</strong></td>
</tr>
</tbody>
</table>
Background

- Proposed as an investigative one year project for CY 2017
- Split into three projects based on request of IAB
  - This project
  - ML design of FPGAs
  - ML in back end design of ASICs
  - i.e. PhD time spent on each project small
  - Did get some assistance from MS students
Problem Statement

• **Boolean Design Rule Checking “broken”**
  o Very complex rule set
  o Back end checking time-consuming, slowing design flow
  o Increasing disconnect to manufacturing

• **Industry relevance:**
  o Speed up design in advanced nodes
  o Potential for better automation in full custom layout
  o Solve DFM productivity gap
Proposed Solution

- Replace Boolean DRC with Neural Networks
- Use Machine-Learning techniques to make sense of complex relationships
- First year experiment:
  - Apply Neural Networks to raw image data
  - 80% recognition rate
- Going forward
  - Improve feature extraction
  - Experiment with different choices for ML model and model setup
Progress to date

- Took ~50 SRAM designs from ECE 546
  - Done in 15 nm PDK
  - Focus M1 width rule
  - Translated to gdt
    - Generated random variants of designs
    - Ran 5,000 samples through DRC to create labeled data
    - Ran a scan window to produce 5 million images
  - Demonstrate that DRC can be done with trained ML models

Original Layout

Variation #1

Variation #2
**Trained a Neural Network with 20,000 random images**
- Two layer network
- TensorFlow using tflearn/keras API
- Rectified Linear Unit (ReLU) activation function
- Learning rate set to 0.001
- Takes only a few minutes to train
- Achieved 80% recognition rate on retained images
Project Objectives

• **Demonstrate that DRC can be done with trained ML models**
  - Based on extracted features
  - Experiment with different networks
  - Increase amount of data

• **After success with training**
  - Expand rule set to full 15 nm PDK
  - Investigate connection to yield monitor data

• **In year 2:**
  - Investigate deriving rules from yield monitor data, OR
  - Investigate driving semi-automated layout
Technical Approach (Year 1)

• Work on extracted features, not raw pixelated image data
  o E.g. layout shape coordinates
  o Greatly reduces data set size
  o Likely to increase success rate

• Increase training set

• Investigate different networks and parameters

• Extend to other rules
Technical Approach (Year 2)

- **Investigate connection to yield monitors**
  - Train same networks from yield monitors, instead of labelled DRC rules
  - OR
- **Investigate driving layout**
  - Treat layout as a parameterized model
## Annual Milestones

<table>
<thead>
<tr>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jan 1</td>
<td>Project Start</td>
</tr>
<tr>
<td>Apr 30</td>
<td>Fit Model for one design including Power-Rail &amp; Clock-Tree Insertion</td>
</tr>
<tr>
<td>Sep 30</td>
<td>Fit Models for all benchmark circuits</td>
</tr>
<tr>
<td>Dec 31</td>
<td>Analysis of Classification Criteria Demonstration of Productivity Gain on One Design</td>
</tr>
</tbody>
</table>
Deliverables and Outcomes

• Year 1
  o (Outcome) Demonstrated improved recognition rate
  o (Outcome) Then expand to more complete rule set
  o (Deliverables) Reports on outcomes and sample code

• Year 2
  o (Outcome) Investigate learning from yield monitors
  o Investigate driving layout with machine learning
    ▪ Parameterized layout generators
Collaborators and Resources

- **Collaborators:**
  - NCSU project

- No additional resources required
## Proposed Budget

<table>
<thead>
<tr>
<th>Category</th>
<th>Number</th>
<th>Cost (per year)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grad. students</td>
<td>12 months</td>
<td>$26,000</td>
</tr>
<tr>
<td>Faculty support</td>
<td>0.5 months</td>
<td>$3,000</td>
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<tr>
<td>Benefits</td>
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<td>$6,600</td>
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<tr>
<td>Travel</td>
<td>3 trips</td>
<td>$5,000</td>
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<tr>
<td>Indirect costs</td>
<td>10% rate</td>
<td>$4,160</td>
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<tr>
<td>Tuition waivers</td>
<td># of GRAs</td>
<td>$17,559</td>
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<tr>
<td>TOTAL</td>
<td></td>
<td><strong>$53,926</strong></td>
</tr>
</tbody>
</table>
COFFEE BREAK
10:00 – 10:15
LIFE Form Discussion on the eight New and Follow-on Proposals

Led by D. Becker & D. Hoffman, Attendance restricted to Site Directors, NSF & IAB

10:15 – 11:45
Working Lunch by IAB and discussion and voting for Y2 projects

Led by D. Becker & D. Hoffman,
Attendance restricted NSF & IAB
11:45 am
Center Wide Meeting
Led by D. Becker & E. Rosenbaum
1:45 pm – 2:15
AGENDA

• What is the proper engagement for mentors?
• Review of this meetings format
  o What went well?
  o What needs to change for next time?
• Other topics
IAB Report Out, Action items and plans for next meeting

Attendance restricted to Site Directors, NSF & IAB
2:15-2:45
Summary and Closing Remarks
2:45 – 3:00
Thank you for being here

We appreciate you sharing your time and expertise to make CAEML successful