WELCOME

Industry members, students and faculty, welcome to the October 2017 semiannual meeting of CAEML!

It’s been one year since the center’s kick-off and 10 months since the research commenced. Over the next one and a half days, attendees will have the opportunity to review the research progress and results, advise one another, and share ideas. We urge you to keep those conversations going after the review. To facilitate that, you will find enclosed contact information for all attendees.

We will get to hear presentations on eight very interesting new research proposals. During a closed-door session, the IAB and site directors will discuss recent progress on new member recruitment. This is an important subject since the addition of new members will allow CAEML to support more research projects. Time permitting, the site directors would also like to start a conversation about future requests for proposals, e.g., the format and timing. It’s going to be a busy one-and-a-half days but we are confident that each of us will return home excited about the Center and its work.

We want to extend a special welcome to new attendees: professors who are seeking to join the CAEML research team and any engineers from the member companies who did not attend the earlier meetings. Finally, we’d like to offer special thanks to the NCSU staff; their advance planning and hard work will make the meeting a logistical success.

Elyse Rosenbaum
Center Director, University of Illinois at Urbana-Champaign

Paul Franzon
Site Director, North Carolina State University

Madhavan Swaminathan
Site Director, Georgia Tech
# AGENDA

**James B. Hunt Jr. Centennial Campus Library Rooms A & B**  
**Thursday, October 12, 2017**

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
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<tbody>
<tr>
<td>7:15 AM</td>
<td>Registration, Continental Breakfast, and Networking Time</td>
</tr>
<tr>
<td>8:00 AM</td>
<td>Welcoming Remarks</td>
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<tr>
<td>8:15 AM</td>
<td>Introduction of attendees</td>
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<tr>
<td>8:30 AM</td>
<td>Presentation by NSF Assessment Coordinator Dee Hoffman</td>
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<tr>
<td>9:30 AM</td>
<td>State of Center Report</td>
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<td>9:45 AM</td>
<td>Closed door IAB meeting</td>
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<td>1. By-Laws Approval</td>
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<tr>
<td>10:30 AM</td>
<td>COFFEE BREAK</td>
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<td>10 minute presentation, 5 minutes LIFE form completion</td>
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<tr>
<td>11:00 AM</td>
<td>1A2 Quad Chart Report &amp; Y2 Proposal: Intellectual Property Reuse through Machine Learning</td>
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<td>10 minute presentation, 5 minutes LIFE form completion</td>
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<tr>
<td>11:15 AM</td>
<td>1A4 Quad Chart Project Final Report: Design Rule Checking with Deep Networks</td>
</tr>
<tr>
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<td>5 minute presentation, 5 minutes LIFE form completion</td>
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<tr>
<td>11:25 AM</td>
<td>1A5 Quad Chart Report &amp; Y2 Proposal: Behavioral Model Development for High-Speed Links</td>
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<td>15 minute presentation, 5 minutes LIFE form completion</td>
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<tr>
<td>11:45 AM</td>
<td>1A6 Quad Chart Report &amp; Y2 Proposal: Models to Enable System-level Electrostatic Discharge Analysis</td>
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<td>10 minute presentation, 5 minutes LIFE form completion</td>
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<tr>
<td>12:00 PM</td>
<td>1A7 Quad Chart Report &amp; Y2 Proposal: Optimization of Power Delivery Networks for Maximizing Signal Integrity</td>
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<td>10 minute presentation, 5 minutes LIFE form completion</td>
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<tr>
<td>12:15 PM</td>
<td>Lunch &amp; Project Report Poster Session</td>
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<tr>
<td>2:00 PM</td>
<td>LIFE Form completion for all project reports</td>
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<td>20 minute presentation, 5 minutes Q&amp;A, 5 minutes LIFE form completion</td>
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<td>20 minute presentation, 5 minutes Q&amp;A, 5 minutes LIFE form completion</td>
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AGENDA

3:45 PM  New Project Proposal 2A4: Machine Learning to Predict Successful FPGA Compilation Strategy | S. Lim  
20 minute presentation, 5 minutes Q&A, 5 minutes LIFE form completion

4:15 PM  LIFE Form Discussion for Five Renewal Proposals from morning session  
Led by D. Becker & D. Hoffman, Attendance restricted to Site Directors, NSF and IAB

4:45 PM  Proposal Poster Session – All project proposals; renewal, new and follow on

6:30 PM  Cocktails and Dinner  
Dorothy and Roy Park Alumni Center

Engineering Building II Room 3001  
Friday, October 13, 2017

7:15 AM  Registration, Continental Breakfast, and Networking Time

8:00 AM  Follow-on Project Proposal 2A5: Applying Machine Learning to FPGA Design | P. Franzon & R. Davis  
20 minute presentation, 5 minutes Q&A, 5 minutes LIFE form completion

8:30 AM  New Project Proposal 2A6: Causal Inference for Early Detection of Hardware Failure | N. Kiyavash, M. Raginsky & E. Rosenbaum  
20 minute presentation, 5 minutes Q&A, 5 minutes LIFE form completion

9:00 AM  Follow-on Project Proposal 2A7: Applying Machine Learning to Back End IC Design | R. Davis & P. Franzon  
20 minute presentation, 5 minutes Q&A, 5 minutes LIFE form completion

9:30 AM  Follow-on Project Proposal 2A8: Applying Machine Learning to Design Rule Checking | P. Franzon & R. Davis  
20 minute presentation, 5 minutes Q&A, 5 minutes LIFE form completion

10:00 AM  COFFEE BREAK

10:15 AM  LIFE form review and discussion for eight New and Follow-on Proposals  
Led by D. Becker & D. Hoffman, Attendance restricted to Site Directors, NSF and IAB

11:45 AM  Working lunch by IAB discussion and voting for Y2 project funding

12:45 PM  Discussions and voting continue until complete

1:45 PM  Center wide meeting  
1. What is the proper engagement for mentors  
2. Review of this meeting’s format – what went well, what needs to change for next time?  
3. Other topics

2:15 PM  IAB Report out, Action items and plans for next meeting  
Attendance restricted to Site directors, NSF, IAB

2:45 PM  Summary, Closing and Adjournment  
E. Rosenbaum & D. Becker
CAEML RESEARCH LEADERS

Dror Baron
dee.ncsu.edu/people/dzbaron
Dror Baron received the B.Sc. (summa cum laude) and M.Sc. degrees from the Technion - Israel Institute of Technology, Haifa, Israel, in 1997 and 1999, and the Ph.D. degree from the University of Illinois at Urbana-Champaign in 2003, all in electrical engineering.

From 1997 to 1999, he was a Modem Designer at Witcom Ltd. From 1999 to 2003, he was a Research Assistant at the University of Illinois at Urbana-Champaign, where he was also a Visiting Assistant Professor in 2003. From 2003 to 2006, he was a Postdoctoral Research Associate in the Department of Electrical and Computer Engineering at Rice University, Houston, TX. From 2007 to 2008, he was a Quantitative Financial Analyst with Menta Capital, San Francisco, CA. From 2008 to 2010 he was a Visiting Scientist in the Electrical Engineering Department at the Technion. Dr. Baron joined the Department of Electrical and Computer Engineering at North Carolina State University in 2010, and is currently an associate professor. His research interests include information theory and statistical signal processing.

Deming Chen
dchen.ece.illinois.edu/
Dr. Deming Chen obtained his BS in computer science from University of Pittsburgh, Pennsylvania in 1995, and his MS and PhD in computer science from University of California at Los Angeles in 2001 and 2005 respectively. He worked as a software engineer between 1995-1999 and 2001-2002. He joined the ECE department of University of Illinois at Urbana-Champaign (UIUC) in 2005 and has been a full professor in the same department since 2015. He is a research professor in the Coordinated Science Laboratory and an affiliate professor in the CS department. His current research interests include system-level and high-level synthesis, computational genomics, GPU and reconfigurable computing, and hardware security. He has given more than 90 invited talks sharing these research results worldwide. Dr. Chen is a technical committee member for a series of top conferences and symposia on EDA, FPGA, low-power design, and VLSI systems design. He also served as Program or General Chair, TPC Track Chair, Session Chair, Panelist, Panel Organizer, or Moderator for many of these conferences. He is an associate editor for several IEEE and ACM journals. He received the NSF CAREER Award in 2008. He received the ACM SIGDA Outstanding New Faculty Award in 2010, and IBM Faculty Award in 2014 and 2015. He also received six Best Paper Awards. He is included in the List of Teachers Ranked as Excellent in 2008. He was involved in two startup companies previously, which were both written more than 250 papers. He joined the faculty at Illinois in 1997. He is the M.E. Van Valkenburg Professor in Electrical and Computer Engineering and served as the head of the department from 2008 to 2013. He was an Associate Provost Fellow on the Urbana campus from 2006 to 2008. He is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE), and the recipient of a Humboldt Foundation Research Award, the U.S. Army Research Laboratory Director’s Coin, and the IEEE Microwave Theory & Techniques Distinguished Educator Award.
acquired. In 2016, he co-founded a new startup, Inspirit IoT, Inc., for design and synthesis for machine learning targeting the IoT industry. He is the Donald Biggar Willett Faculty Scholar of College of Engineering of UIUC.

**Rhett Davis**  
[ecn.ncsu.edu/people/wdavis](ecn.ncsu.edu/people/wdavis)  
W. Rhett Davis is a Professor of Electrical and Computer Engineering at North Carolina State University. He received B.S. degrees in electrical engineering and computer engineering from North Carolina State University, Raleigh, in 1994 and M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley in 1997 and 2002, respectively. He received the National Science Foundation’s Faculty Early Career Development (CAREER) award in 2007, and received the Distinguished Service Award from the Silicon Integration Initiative (Si2) in 2012 for his research in the development of standards for electronic design automation (EDA) and his development of the FreePDK open-source, predictive process design kit. He is working with Si2 to develop standards for system-level power modeling and compact modeling of device reliability. He has been an IEEE member since 1993 and a Senior Member since 2011. He has published over 50 scholarly journal and conference articles. He has worked at Hewlett-Packard (now Keysight) in Boeblingen, Germany and consulted for Chameleon Systems, Qualcomm, BEECube, and Silicon Cloud International. Dr. Davis’s research is centered on electronic design automation for integrated systems in emerging technologies. He is best known for his efforts in design enablement, 3DIC design, thermal analysis, circuit simulation, and power modeling for systems-on-chip and chip multiprocessors.

**Brian Floyd**  
[people.engr.ncsu.edu/bafloyd](people.engr.ncsu.edu/bafloyd)  
Brian Floyd received the B.S. with highest honors, M. Eng., and Ph.D. degrees in electrical and computer engineering from the University of Florida, Gainesville in 1996, 1998, and 2001, respectively. From 2001 to 2009, he worked at the IBM T. J. Watson Research Center in Yorktown Heights, New York, first as a research staff member and then later as the manager of the millimeter-wave circuits and systems group. His work at IBM included the development of silicon-based millimeter-wave transceivers, phased arrays, and antenna-in-package solutions. In 2010, Dr. Floyd joined the Department of Electrical and Computer Engineering at North Carolina State University as an Associate Professor. His research interests include RF and millimeter-wave circuits and systems for communications, radar, and imaging applications.

Dr. Floyd has authored or co-authored over 90 technical papers and has 25 issued patents. He was an Associate Editor for the IEEE Journal of Solid-State Circuits and has served on the technical program committee for the IEEE International Solid-State Circuits Conference (ISSCC). He currently serves on both the steering and technical program committees for the IEEE RFIC Symposium. From 2006 to 2009, he served on the technical advisory board of the Semiconductor Research Corporation (SRC) integrated circuits and systems science area, and currently serves as a thrust leader for the SRC’s Texas Analog Center of Excellence. He received the 2016 NC State Outstanding Teacher Award, the 2015 NC State Chancellor’s Innovation Award, the 2014 IBM Faculty Award, the 2011 DARPA Young Faculty Award, the 2004 and 2006 IEEE Lewis Winner Awards for best paper at the International Solid-State Circuits Conference, and the 2006 and 2011 Pat Goldberg Memorial Awards for the best paper within IBM Research.

**Paul Franzon**  
[ecn.ncsu.edu/erl/faculty/paulf](ecn.ncsu.edu/erl/faculty/paulf)  
Paul D. Franzon is currently a Cirrus Logic Distinguished Professor of Electrical and Computer Engineering and Director of Graduate Programs at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Australia. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom, and three companies he cofounded: Communica, LightSpin Technologies, and Polymer Braille Inc. His current interests center on the technology and design of complex microsystems incorporating VLSI, MEMS, advanced packaging, and nano-electronics. He has led several major efforts and published over 300 papers in those areas. In 1993, he
received an NSF Young Investigators Award; in 2001, he was selected to join the NCSU Academy of Outstanding Teachers; and in 2003, he was named an Alumni Undergraduate Distinguished Professor. He received the Alcoa Research Award in 2005, and the Board of Governors Teaching Award in 2014. He served with the Australian Army Reserve for 13 years as an Infantry Soldier and Officer. He is a Fellow of the IEEE.

Chuanyi Ji
jic.ece.gatech.edu

Chuanyi Ji's research is in large-scale networks, machine learning, and big data sets. She received a B.S. degree from Tsinghua University, Beijing, China, in 1983, an M.S. degree from the University of Pennsylvania, Philadelphia in 1986, and a Ph.D. degree from the California Institute of Technology, Pasadena in 1992, all in Electrical Engineering. She was an Assistant and Associate Professor from 1991 to 2001 at the Rensselaer Polytechnic Institute (RPI), Troy, NY. She was a visitor/consultant at Bell Labs Lucent, Murray Hill, NJ in 1999, and a visiting faculty member at the Massachusetts Institute of Technology, Cambridge in 2000. She is an Associate Professor with the Georgia Institute of Technology, Atlanta, which she joined in 2001. Dr. Ji's awards include a CAREER award from NSF and an Early CAREER award from RPI. She was a co-founder of a startup company on network monitoring and management.

Sung-Kyu Lim
ece.gatech.edu/faculty-staff-directory/sung-kyu-lim

Sung Kyu Lim received the B.S., M.S., and Ph.D. degrees from the University of California at Los Angeles in 1994, 1997, and 2000, respectively. He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology in 2001, where he is currently Dan Fielder Endowed Chair Professor. His current research interests include modeling, architecture, and electronic design automation (EDA) for 3D ICs. His research on 3D IC reliability is featured as Research Highlight in the Communication of the ACM in 2014. His 3D IC test chip published in the IEEE International Solid-State Circuits Conference (2012) is generally considered the first multi-core 3D processor ever developed in academia. Dr. Lim is a recipient of the National Science Foundation Faculty Early Career Development (CAREER) Award in 2006. He received the Best Paper Awards from the IEEE Asian Test Symposium (2012) and the IEEE International Interconnect Technology Conference (2014). He has been an Associate Editor of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) since 2013. He received the Class of 1940 Course Survey Teaching Effectiveness Award from Georgia Institute of Technology (2016).

Maxim Raginsky
csl.illinois.edu/directory/faculty/maxim

Maxim Raginsky received B.S. and M.S. degrees in 2000 and a Ph.D. degree in 2002 from Northwestern University, all in Electrical Engineering. He has held research positions with Northwestern, the University of Illinois at Urbana-Champaign (where he was a Beckman Foundation Fellow from 2004 to 2007), and Duke University. In 2012, he returned to UIUC, where he is currently an Associate Professor and William L. Everett Fellow with the Department of Electrical and Computer Engineering, and a member of the Decision and Control Group in the Coordinated Science Laboratory. His research interests include understanding, modeling, and analyzing complex systems that have capabilities for sensing, communication, adaptation, and decision-making and that can operate effectively in uncertain and dynamic environments. His research examines new angles and perspectives between machine learning, control, optimization, and information theory.

Arijit Raychowdhury
ece.gatech.edu/faculty-staff-directory/arijit-raychowdhury

Arijit Raychowdhury (M-’07, SM-’13) is currently an Associate Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology where he currently holds the ON Semiconductor Junior Research Professorship. He received
his Ph.D. degree in Electrical and Computer Engineering from Purdue University and his B.E. in Electrical and Telecommunication Engineering from Jadavpur University, India. He joined Georgia Tech in January, 2013. His industry experience includes five years as a Staff Scientist in the Circuits Research Lab, Intel Corporation and a year as an Analog Circuit Designer with Texas Instruments Inc. His research interests include digital and mixed-signal circuit design, design of on-chip sensors, memory, and device-circuit interactions.

Dr. Raychowdhury holds more than 25 U.S. and international patents and has published over 100 articles in journals and refereed conferences. He is the winner of the NSF CRII Award, 2015; Intel Labs Technical Contribution Award, 2011; Dimitris N. Chorafas Award for outstanding doctoral research, 2007; the Best Thesis Award, College of Engineering, Purdue University, 2007; Best Paper Awards at the International Symposium on Low Power Electronic Design (ISLPED) 2012, 2006; IEEE Nanotechnology Conference, 2003; SRC Technical Excellence Award, 2005; Intel Foundation Fellowship 2006, NASA INAC Fellowship 2004, and the Meissner Fellowship 2002. Dr. Raychowdhury is a Senior Member of the IEEE.

Dr. Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. She received the B.S. degree (with distinction) from Cornell University in 1984, the M.S. degree from Stanford University in 1985, and the Ph.D. degree from the University of California, Berkeley in 1992, all in electrical engineering. From 1984 through 1987, she was a Member of Technical Staff at AT&T Bell Laboratories in Holmdel, NJ.

Dr. Rosenbaum’s present research interests include component and system-level ESD reliability, ESD-robust high-speed I/O circuit design, compact modeling, mitigation strategies for ESD-induced soft failures, and machine-learning aided behavioral modeling of microelectronic components and systems. She has authored nearly 200 technical papers. From 2001 through 2011, she was an editor for IEEE Transactions on Device and Materials Reliability. She is currently an editor for IEEE Transactions on Electron Devices. Dr. Rosenbaum is the General Chair for the 2018 International Reliability Physics Symposium.

Dr. Rosenbaum was the recipient of a Best Student Paper Award from the IEDM, as well as Outstanding and Best Paper Awards from the EOS/ESD Symposium. She has received an NSF CAREER award, an IBM Faculty Award, and the ESD Association’s Industry Pioneer Recognition Award. Dr. Rosenbaum is a Fellow of the IEEE.

José Schutt-Ainé received a B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC) in 1984 and 1988, respectively. He was an Application Engineer at the Hewlett-Packard Technology Center, Santa Rosa, CA, where he was involved in research on microwave transistors and high-frequency circuits. In 1983, he joined UIUC, and then joined the Electrical and Computer Engineering Department and became a member of the Electromagnetics and Coordinated Science Laboratories. He is a consultant for several corporations. His current research interests include the study of signal integrity and the generation of computer-aided design tools for high-speed digital systems. Dr. Schutt-Ainé is the recipient of several research awards, including the 1991 National Science Foundation (NSF) MRI Award, the National Aeronautics and Space Administration Faculty Award for Research (1992), the NSF MCAA Award (1996), and a UIUC National Center for Supercomputing Applications Faculty Fellow Award (2000). He is an IEEE Fellow and is currently serving as Co-Editor-in-Chief of the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT).
Madhavan Swaminathan

c3ps.gatech.edu; epsilonlab.ece.gatech.edu

Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE) and Director of the Center for Co-Design of Chip, Package, System (C3PS), Georgia Tech. He formerly held the position of Joseph M. Pettit Professor in Electronics in ECE and Deputy Director of the NSF Microsystems Packaging Research Center, Georgia Tech. Prior to joining Georgia Tech, he was with IBM working on packaging for supercomputers. He is the author of 450+ refereed technical publications, holds 29 patents, is primary author and co-editor of 3 books, and was founder and co-founder of two start-up companies (E-System Design and Jacket Micro Devices) and founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the CPMT society on Signal Integrity in the Asian Region. He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE EMC society. He received his M.S. and Ph.D. degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.

Shobha Vasudevan

faculty.ece.illinois.edu/shobhav/

Shobha Vasudevan is an associate professor at the Electrical and Computer Engineering department at the University of Illinois at Urbana-Champaign. Her research interests are in system verification and security, analog and digital hardware validation, formal, static analysis and statistical algorithms, machine learning and causal inferencing in big data and biomedical device modeling. Her research software for automatic assertion generation, GoldMine, is being licensed by several companies including IBM, AMD, Qualcomm, Huawei Technologies, TI, Oracle, and is being developed by a leading EDA company into a commercial product. She is a technical consultant for several companies. She is the recipient of the Best Paper Award in DAC 2014, NSF CAREER award, the ACM SIGDA outstanding new faculty award, the Dean’s Award for Excellence in Research, Best paper award in VLSI Design 2014, IEEE Council of EDA Early Career Award, the YWCA award for mentoring women, IBM faculty partnership award 2017 and several best paper nominations. She is a senior member of the IEEE and serves as associate editor of IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems.


## Project Proposals

### Project Summary

**Title:** Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems  
**Date:** 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Tracking No.:** 1A1  
**Project Leader(s):** Maxim Raginsky (UIUC) and Andreas Cangellaris (UIUC)

**Phone(s):** (217) 244-1782  
**E-mail(s):** maxim@illinois.edu, cangella@illinois.edu

**Proposed Budget:** $96k  
**Type:** Continuing

**Other Faculty Collaborator(s):** Chuanyi Ji (Georgia Tech)

### Project Description

The project focuses on theoretical foundations and modular algorithmic solutions for ML-driven design, simulation, and verification of high-complexity, multifunctional electronic systems. Behavioral system modeling provides a systematic approach to reconciling the variety of physics-based and simulation-based models, expert knowledge, and other possible means of component description commonly introduced in electronic systems modeling. In complex electronic systems, each component model comes with its own sources of errors, uncertainty, and variability, and the same applies to the way components and subsystems are connected and interact with each other in the integrated system. The modularity offered by the behavioral approach will be leveraged to develop mathematical tools for assessing the performance and minimal data requirements for learning a low-complexity representation of the system behavior, one component or subsystem at a time, from measured and simulated data even in highly complex and uncertain settings. We will develop and implement the full ML algorithmic pipeline and quantify its end-to-end performance in applications pertinent to multifunctional electronic system design, simulation, and verification.

### Progress to Date (if applicable)

1. Analyzed local and global stability of gradient descent with backpropagation, the standard method for training complex nonlinear models, such as neural networks.  
2. Developed methodology for learning stable recurrent neural network models that compose well with circuit simulators.  
3. Developed methodology for integrating flexible probabilistic generative models into passive macromodeling pipeline.

### Experimental plan (current year only)

In the context of behavioral system modeling, both learning algorithms and their outputs are probabilistic programs that consist of deterministic transformations (nominal device models), random variable generators (to capture noise and component/process variability), and probabilistic conditioning (to capture constraints or relations among internal and external variables). Furthermore, significant structural complexity of realistic electronic systems leads to chaotic behavior of the electromagnetic fields responsible for EMI events. As such, in addition to often being computationally prohibitive, a deterministic approach to computer-aided investigation of performance tradeoffs may not be sufficient to inform design decisions. The use of probabilistic program formalism will allow us to develop robust and mathematically sound techniques for capturing all sources of noise and variability in behavioral models and for quantifying the concentration of typical system behavior around the mean or median nominal model. In addition, it will pave the way for more efficient and meaningful predictive EMI analysis at the system level.

### Related work elsewhere and how this project differs

To date, behavioral modeling of electronic systems in the presence of uncertainty/variability is dominated by approaches that propagate the stochastic attributes of any input parameters to the output. In contrast, our method will produce a low-complexity representation of the system behavior from measured and simulated data that lends itself to expedient, yet accurate simulation.

### Proposed milestones for the current year

1. Theoretical and algorithmic framework for modular ML  
2. Identify test structure for system-level EMI modeling.

### Proposed deliverables for the current year

1. Design and characterization of each element of the ML pipeline as a probabilistic program, including tools for uncertainty quantification in behavioral models.  
2. Report on the application of probabilistic modeling to expedite EMI modeling and simulation of realistic electronic systems.

### Potential Member Company Benefits

System designers are confronting increasing demands on end-to-end system functionality integration and resilience, while facing competitive time-to-market and low-cost constraints. The increased complexity of these systems hinders high-fidelity predictive modeling and performance simulation, which, in turn, may lead to overly conservative designs that unnecessarily sacrifice performance and even increase cost. This project will tackle these pressing industry challenges.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/18
### Project Summary

**Title:** Intellectual Property Reuse Through Machine Learning  
**Date:** 9/1/17

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<th><strong>Center:</strong></th>
<th>Center for Advanced Electronics through Machine Learning (CAEML)</th>
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<tr>
<td><strong>Tracking No.:</strong></td>
<td>1A2</td>
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<tr>
<td><strong>Project Leader(s):</strong></td>
<td>Franzon/Floyd (NCSU)</td>
</tr>
<tr>
<td><strong>Phone(s):</strong></td>
<td>(919) 515-7351</td>
</tr>
<tr>
<td><strong>E-mail(s):</strong></td>
<td>{paulf, bafloyd}@ncsu.edu</td>
</tr>
<tr>
<td><strong>Proposed Budget:</strong></td>
<td>$64,155</td>
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**Other Faculty Collaborator(s):** Baron (NCSU)

**Project Description:** The objective of this project was to demonstrate that machine learning can be applied to the problem of recasting an analog or full custom digital design from one technology node to another, assuming the same circuit topology.

**Progress to Date (if applicable):** A Bayesian optimization framework was put together to tackle this problem. It builds a coarse surrogate model of the design and then conducts screening on the design in order to reduce the number of design dimensions. Bayesian optimization is then used to find the optimal point in the new technology with the minimum number of iterations. A webinar was given on the tool and the underlying methods in August 2017. To date the tool has been demonstrated on a Balun and power amplifier circuit. The resulting designs were better than the human generated ones.

**Experimental plan (current year only):** We will demonstrate the design on a mixer and a serdes receiver. The receiver includes PLL, CTLE and DFE stages. As well as demonstrating the tool on each of the stages, we will demonstrate a new capability that considers tradeoff between the stages. This will be done using the surrogate models for the different stages together in an optimization tradeoff analysis. Different optimization strategies will be investigated. In addition, we will complete the measurement comparisons on the RF circuit blocks.

**Related work elsewhere and how this project differs:** Not aware of directly related work.

**Proposed milestones for the current year:** (1) Completion of Mixer design; (2) Design comparison with measurement; (3) Investigation for optimization of individual blocks in SerDes; (4) Investigation of co-optimization of blocks in SerDes.

**Proposed deliverables for the current year:** Demonstration and reports associated with these milestones. The tool has already been delivered to the Center for member distribution.

**Projected deliverables for Year 2 (if applicable):**

**Potential Member Company Benefits:** Improved ability to achieve optimal designs for analog and full custom blocks with a fixed circuit topology across different circuit nodes.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/18
# Project Summary

**Title:** Behavioral Model Development for High-Speed Links  
**Date:** 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

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<td><strong>Project Leader(s):</strong></td>
<td>Madhavan Swaminathan (GT), José Schutt-Aíné (UIUC), and Prof. Paul Franzon (NCSU)</td>
</tr>
<tr>
<td><strong>Phone(s):</strong></td>
<td>(404) 227-0087</td>
</tr>
<tr>
<td><strong>E-mail(s):</strong></td>
<td><a href="mailto:madhavan@ece.gatech.edu">madhavan@ece.gatech.edu</a>; <a href="mailto:josec@emlab.illinois.edu">josec@emlab.illinois.edu</a>; <a href="mailto:paulf@ncsu.edu">paulf@ncsu.edu</a></td>
</tr>
<tr>
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**Other Faculty Collaborator(s):** Chuanyi Ji (GT) and Maxim Raginsky (UIUC)

## Project Description

High-speed links consist of driver and receiver circuits connected to through interconnections in the chip, package, and printed circuit board. Over several decades, as the speed of the channel has increased, the driver and receiver circuits have become quite complex to compensate for any shortcomings of the channel; e.g., they contain pre-distortion, pre-emphasis, adaptive control, and equalization circuitry. This project’s goal is to apply machine-learning methods to systematically develop a hierarchy of behavioral models of circuits that have the same accuracy as the transistor-level models, but require 25–50X less CPU time and memory. The behavioral models will be suitably parameterized to include a range of channel conditions that can be used for design verification and optimization. Three approaches will be used: 1) using time-domain data, 2) using X-parameters, and 3) building receiver models using system identification and surrogate modeling. We will compare the three approaches as part of this project.

**Progress to Date (if applicable):** We have developed behavioral models for fixed frequency oscillators and VCOs using neural networks (~10X faster than transistor models), based on collaboration with Cadence. This has resulted in an accepted paper at EPEPS ‘17 conference. We are currently collaborating with Qualcomm on behavioral modeling of I/O drivers using RNN and with IBM on HSSCDR modeling. We have completed Volterra kernel (VK) extraction using a second-order approximation. This extraction can be performed from harmonic balance (HB) simulation or using X-parameters. This work has led to a paper that will be presented at the RADIO-17 conference. Using higher orders will necessitate a tensor representation to handle the large amount of X-parameter data. The data and algorithm will be used to train an ANN and automate the kernel generation process. For receiver modeling, the main outcome to date has been the identification of the Neural Network ARMAX modeling technique as one that gives high predictive accuracy for RXs using DFE and CTLE.

**Experimental plan (current year only):** Behavioral Modeling using Time Domain Data: The waveforms for training will be obtained from simulation (or measurement) of the transistor-level circuits. 1) Georgia Tech students have received training to use IBM’s HSSCDR tool where concepts and notations of high-speed channel design as well as syntax of HSSCDR tool have been presented for generating channels with different interconnect characteristics with emphasis on insertion loss, crosstalk, optimal equalization settings and analysis of eye diagrams. Data generated from this tool will be used for generating time-domain channel response using input-output waveforms and s-parameters. 2) We will explore algorithms that minimize the number of training data sets required by incorporating expert ML methods that can lead to automation for the generation of the training data sets where RNN based methods will be investigated. Behavioral Modeling using X-Parameter Data: Our efforts will focus on evaluating and validating the second-order VK. The device under test will be a buffer of CMOS type. X-parameter data will be obtained (a) from harmonic balance simulation using ADS and (b) from measurement using a nonlinear vector network analyzer (NVNA). The data obtained will be used to train an ANN into generating the kernels. We plan to demonstrate a prototype of this neuro-VK based simulation tool for a high-speed link driver and comparing the results with those of traditional IBIS simulations. Receiver Modeling: Demonstration of ability to model a measured receiver and a simulated one. Delivery of code that could be ported to an oscilloscope. Methods will be investigated to classify system noise so the impact of PSIIJ can be predicted.

**Related work elsewhere and how this project differs:** This is based on earlier work the investigators did in the area of recurrent neural networks, identification modeling, surrogate modeling, and X-parameters. Opportunities exist to enable a high degree of automation in the model development process because of the advancements in ML algorithms.

**Proposed milestones for the current year:** Perform benchmark test with IBIS (Volterra); Software that uses machine learning for the generation of behavioral models for circuits used in high-speed signaling; Comparison of results for accuracy and speed (transistor circuits and IBIS); Implement x2ibis; Merge x2ibis and ML-Volterra methods; Automated software for behavioral model and SPICE netlist generation; Comparison of ML-based methods along with documentation for model development; Technology transfer through internships.

**Proposed deliverables for the current year:** Software that automates the behavioral model construction and SPICE netlist generation. Application to high-speed channels with 10–20 ports. Demonstration of 25X–50X speed-up. Predict transient voltage and currents at input and output of simulator. Complete RX modeling extraction. Comparison between the methods developed for determining best technique for a class of circuitry.

**Potential Member Company Benefits:** Accurate SPICE models with 25–50X reduction in simulation time.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** Dec. 31, 2018
**Project Summary**  
**Title:** Models to Enable System-level Electrostatic Discharge Analysis  
**Date:** 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)  
**Tracking No.:** 1A6  
**Project Leader(s):** Elyse Rosenbaum (UIUC); Maxim Raginsky (UIUC)  
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**Proposed Budget:** $63,902  
**Type:** Continuing  
**Other Faculty Collaborator(s):** Madhavan Swaminathan (GT)

**Project Description:** Statistical learning is used to create models for system-level ESD simulation. Primarily, the models are for the nonlinear components of the system. Domain expertise is employed to select an appropriate class of model functions. The models are targeted for circuit or hybrid (EM-circuit) simulators. The simulation results reveal whether the ESD-induced current and voltage waveforms appearing at the terminals of the semiconductor components inside the system will exceed safe limits. If the ESD-induced electrical noise is below damage levels, generative models predict the likelihood that soft errors occur.

**Progress to Date:** The following have been developed. (1) I-V models for I/O pins that are relevant at ESD current levels under both power-on and power-off conditions; these multi-port models capture the multitude of current return paths. (2) RNN models for transient simulation of I/O pin response to ESD. By construction, the RNN model accurately represents the thermal equilibrium condition. The loss function used during training is designed to penalize unstable solutions. The RNN is implemented in Verilog-A and may be used in a variable time-step simulation. (3) Generative model for air discharge waveforms: \( P(X_1, X_2, Y_1, Y_2, Y_3) \), where \( X_1 \) is pre-charge voltage of the ESD source, \( X_2 \) is the speed at which the source approaches the equipment under test (EUT), \( Y_1 \) is the peak ESD current, \( Y_2 \) is the ESD pulse risetime, and \( Y_3 \) is the total charge transferred to the EUT. Bayesian inference is used to approximate the posterior distribution function; kernel density estimation is used to obtain the prior and likelihood distributions.

**Experimental plan (current year only):** Benchmark 4 ESD simulation approaches against measurement data: circuit simulation vs. hybrid EM-circuit simulation; RNN transient models of the components vs. I-V models. Evaluate the feasibility of a more complex return-path model. Presently, all pins within a single net are lumped together for computational efficiency. Separating these pins would allow one to simulate noise coupling inside the package, which is a significant cause of ESD-induced soft-failures. Include additional features (inputs) in the generative model for air discharge; these features should describe the physical design of the EUT, e.g. its dimensions. Improve the dynamic range of the RNN circuit model (making it suitable for AC as well as transient simulations) by using additional inputs during training. Explore other applications of the models developed in this project. RNN models of circuits used in mixed-signal systems will be implemented using Verilog-AMS; the model accuracy and efficiency will be compared to behavioral models used more typically.

**Related work elsewhere and how this project differs:** Work elsewhere (e.g., Univ. Toulouse, imec, Missouri S&T) has focused solely on hard-failure prediction and primarily utilizes single-port static I-V models. Transient simulations have been accurate only in cases where the transient response at an IC port is dominated by the inductive elements in the package. The proposed work avoids oversimplifying the models, resulting in higher fidelity simulation results and the capability to predict soft failures. This project uniquely utilizes generative modeling to represent ESD events that are inherently stochastic in nature.

**Proposed milestones for the current year:** (1) Quantify RNN complexity in terms of the (i) number of ports for the circuit being modeled and (ii) number of nodes in the circuit being modeled (if known). (2) Benchmark simulated waveforms against those obtained from measurement. (3) Demonstrate soft failure prediction capability. (4) Implement RNN circuit models using Verilog-AMS and benchmark the simulation results against other behavioral models.

**Proposed deliverables for the current year:** (1) Code (python or Matlab) to learn models from data: multi-port I-V model of I/O pin ESD response, and generative model for air discharge. (2) RNN models with enhanced dynamic range.

**Potential Member Company Benefits:** Provide a time-saving and cost-effective alternative to a hardware-based trial-and-error method to achieve system ESD robustness. The same RNN structure used for ESD response modeling can be used to obtain behavioral models needed for mixed-signal simulation of circuits and systems.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/18
**Project Summary**

**Title:** Optimization of Power Delivery Networks for Maximizing Signal Integrity  
**Date:** 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Tracking No.:** 1A7  
**Project Leader(s):** Madhavan Swaminathan and Chuanyi Ji (GT)

**Phone(s):** (404) 227-0087  
**E-mail(s):** madhavan@ece.gatech.edu, jichuanyi@gatech.edu

**Proposed Budget:** $76.5k  
**Type:** Continuing

**Other Faculty Collaborator(s):** Elyse Rosenbaum, Maxim Raginsky, and Andreas Cangellaris (UIUC)

**Project Description:** Power distribution is a system-level problem in which the contributions from the chip, package, and printed circuit board are equally important. This, when combined with signal lines, can lead to models that can take a long time to simulate. With optimization being an integral part of design, co-optimization of the signal and power delivery network becomes necessary. As the number of control parameters increases, the co-optimization process can be very time-consuming. In addition, accounting for uncertainty of parameters and variation for complex systems can be challenging. The objective of this project is to explore and develop machine learning (ML) based software to optimize the system output response based on a large set of control parameters and compute BER of channels. We will focus on four applications: 1) 3D ICs; 2) Integrated Voltage Regulators (IVR); 3) Wireless Power Transfer (WPT) for IoT and 4) HSSCDR.

**Progress to Date (if applicable):** We have developed an EDA oriented Bayesian Optimization (BO) algorithm called Two-Stage Bayesian Optimization (TSBO) that has outperformed conventional ML & non-ML optimization algorithms. These have been applied to 1) Clock skew minimization of 3D ICs where TSBO resulted in 4.7% and 2.3% improvement in clock skew and temperature gradient with 4X faster convergence; 2) Multi-objective optimization of IVR where 5.3% increase in IVR efficiency, 55.3% reduction in inductor area and 2X faster performance was achieved; 3) System optimization of a WPT system where 79.1% reduction in receiver coil area and 0.8% improvement in system efficiency were achieved compared to hand-tuned designs along with 67.3% reduction in embedded inductor area for buck converter efficiency >90%. Papers were accepted to COMUS ’17, EPEPS ’17 and a paper was submitted to TVLSI.

**Experimental plan (current year only):** The students have received training to use IBM’s HSSCDR tool where concepts and notations of high-speed channel design and syntax of HSSCDR tool have been presented for generating channels with different interconnect characteristics with emphasis on insertion loss, crosstalk, optimal equalization settings and analysis of eye diagrams. We will investigate applying ML approaches to signal integrity analysis of high-speed channels based on data obtained from the HSSCDR tool. An area we will focus on is identifying worst-case channel interconnect characteristics caused by manufacturing deficiencies. The search space of this problem consists of 19 discrete dimensions, spanning over 5 million different combinations for a given channel topology. The goal is to use ML to find worst-case scenario using minimum number of combinations. We will also investigate the application of uncertainty quantification approaches where we will reduce length of the pulse train for eye diagram and BER analysis by applying kernel estimation method on smaller amounts of data. Rather than rely entirely on randomly sampled data for learning to pick the samples, we propose to incorporate prior learning of knowledge, when available, into learning which include: 1) developing a methodology for generating and selecting pertinent training samples, 2) learning from data based on a “lighted” rather than “black” box, and 3) collecting prior knowledge.

**Related work elsewhere and how this project differs:** ML-based Bayesian optimization methods have been applied extensively in neural engineering. Here, we are modifying these methods appropriately for application to EDA. Prior methods have relied on superposed edge response and statistical eye which tend to have limited use and accuracy.

**Proposed milestones for the current year:** Comparison with non-ML methods; Quantify results based on CPU time and convergence; Software (in Matlab) for implementing TSBO and other Bayesian Optimization based approaches that include strategies for uncorrelated and correlated parameters; Uncertainty quantification and prediction of BER through machine learning; Achieve 10X speedup in eye diagram analysis; Technology transfer to industry.

**Proposed deliverables for the current year:** Software for optimization with 10 or more input parameters; Quantification of the scaling of CPU time with increase in input parameters; Uncertainty analysis and prediction of BER.

**Potential Member Company Benefits:** System optimization solutions involving high dimensional problems (>10); accurate estimation of BER by minimizing simulation runs.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** Dec. 31, 2018
## Project Summary

**Title:** Security-centric synthesis and optimization for trusted hardware design  
**Date:** 9/1/17

### Center:
Center for Advanced Electronics through Machine Learning (CAEML)

### Tracking No.: 2A1  
### Project Leader(s): Deming Chen, University of Illinois at Urbana-Champaign

### Phone(s):  
(217 244 3922)  
### E-mail(s): dchen@illinois.edu

### Proposed Budget:  
$60,000 per year  
### Type: (New/Continuing/Follow-up)  
New

### Project Leader(s)"

### Project Description:
Security and trust in integrated circuits (ICs) remain an ongoing concern, as a security breach at the hardware-level exposes even provably secure algorithms and protocols to vulnerabilities. Among the threats that hardware security faces, hardware Trojans and side channel attacks have emerged as major security concerns. Trojans are not only found in consumer grade electronics, but can exist in mission-critical military equipment as well. Recently, a backdoor was discovered in a military grade FPGA that was implemented in the silicon of the chip itself and could be used to extract secrets and even reprogram the device. In this proposal, we propose novel security-centric synthesis and optimization techniques for secure and trusted hardware system design. We achieve this goal through a new design methodology, where the hardware is designed through high-level synthesis (HLS) -- security and trustiness features can be naturally embedded into a high-level program (e.g., C or C++) and then be compiled into hardware description language (e.g., Verilog). HLS has advantages of higher design productivity, better debugging and testing capability, and faster time to market. Making HLS security and trustiness centric is new as well as an open research field.

Previously, we introduced the first HLS flow that produces a security-enhanced hardware design to directly prevent Hardware Trojan Horse (HTH) injection by a malicious foundry [DAC’16]. Through analysis of entropy loss and criticality decay, the presented algorithms implemented efficient information dispersion to counter HTH insertion. Later, we presented the first HLS flow with primary focus on side-channel leakage reduction [ASAP’17]. Minimal security annotation to the high-level C-code is sufficient to perform automatic analysis of security critical operations with corresponding insertion of countermeasures. Although these techniques are effective, they lead to resource overhead, which can be quite high (up to 2-3x larger chip area). We propose the following new strategies to overcome previous weaknesses and in addition, solve several new challenges.

1) Based on a new open-source hardware/software co-design package just released from my group, we will add security and trust as a new dimension in the hardware/software co-design paradigm. Our goal is to generate a Pareto curve that captures the hardware design space along all the major dimensions, such as trustiness, power/energy consumption, area, and cost, which can provide highly valuable guidance for designers to make the right decision for highly secure hardware design given various area/power/cost constraints. Meanwhile, since hardware/software co-design is a classification problem, we will also explore to use a machine learning-guided algorithm for sophisticated hardware/software partitioning decisions.

2) We would explore new architecture-level optimization techniques. These include: a) information dispersion through replication of execution paths (e.g., cipher key separated into sub-segments and distributed among replicated paths), so the device does not expose a single point of vulnerability anymore; b) new scheduling, resource allocation, and binding algorithms during HLS for operations and data mapping onto target architectures to protect against attacks.

3) We will use novel machine learning techniques (e.g., bidirectional LSTM) to evaluate, identify, and assess different and sophisticated attacking strategies/scenarios and come up with counter-mechanism against such attacks.

### Progress to Date (if applicable):

**Experimental plan (current year only):** Will use simulation and FPGA emulation to evaluate the results.

**Related work elsewhere and how this project differs:** Explained in the project description above.

**Proposed milestones for the current year:** Complete task 1 and task 2(a) above.

**Proposed deliverables for the current year:** Report, publication, and secure hardware design methods.

**Projected deliverables for Year 2 (if applicable):** Complete task 2(b) and task 3 above.

**Potential Member Company Benefits:** New methodology for trusted hardware system design

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/19
Project Summary

**Title:** Machine learning for trusted platform design  
**Date:** 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Tracking No:** 2A2  
**Project Leader(s):** Arijit Raychowdhury (GT) & Madhavan Swaminathan (GT)

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**Proposed Budget:** $54,345 (year 1)  
**Type:** (New/Continuing/Follow-up) New

**Other Faculty Collaborator(s):** Chuanyi Ji (GT)

**Project Description:** Several IoT applications are emerging with RF transceivers and Wireless Power Transfer units integrated in a single module. These are smart modules with embedded signal processing. An example of an architectural embodiment is shown in Figure 1 where a single RF carrier is used for bi-directional RF communication and power delivery. Depending on the application, the module may or may not contain an encryption engine (128b AES) for security. Since many of these systems will be autonomous, trusted platforms are required for keeping such objects secure over the product’s lifetime. Such IoT devices are prone to three types of attacks: 1) Side channel attack (SCA) through RF carrier, 2) Power channel attack through power delivery network and 3) EM channel attack through near or far field coupling. Our objective in this project is to use Machine Learning (ML) to i) assess if the system is under attack (ex: identifying constructive and/or destructive links, ii) developing counter measures (ex: shut down the system or modify the security key) and iii) performing i) and ii) in very short time periods (ex: within milli-seconds after the attack occurs).

**Progress to Date (if applicable):** We currently have a prototype of the Wireless Power Transfer (WPT) module functioning at ~1GHz along with models. We also have experience in developing models of RF transceivers and AES (Advanced Encryption Standard) engines. We will use Chip Whisperer board for Power SCA evaluation. We plan to use this prior work to develop data for Machine Learning. In addition, evaluation boards can be used for testing.

**Experimental plan (current year only):** We recognize that model development is hard and model based prediction is computationally difficult due to the high dimensionality of the system. We therefore need to develop models that have high sensitivity to model parameters and have short detection latencies. Our approach therefore is to use Deep Learning techniques that can predict attacks in milli-seconds. We will develop ANN based observers that can be used to monitor internal system states, which allows us to use predictive models and state estimation theory to identify attacks and develop counter measures. As an example, a state estimator (observer) can be trained to detect variations using current and voltage sensors embedded at different points in the power delivery network loop. Changes in the loop’s states can be detected which can be used by the observer to detect attacks.

**Related work elsewhere and how this project differs:** Prior work on security has focused primarily on developing AES engines that are resilient to cyber-attacks. The concept of using an observer is new.

**Proposed milestones for the current year:** Develop ML methods based on both diagnostic and active learning techniques using ANN and Bayesian Inference methods. Apply Deep Learning techniques for detecting minute changes in the system response in milli-seconds.

**Proposed deliverables for the current year:** Models of the system that include RF communication, WPT and security blocks that includes near field coupling through RF coils at ~1GHz using HFSS, ADS and Matlab; Model of observer; Algorithms developed in Matlab for deep learning based on ANN and Bayesian Inference methods; Model based demonstration of identification of cyber-attacks through RF, Power and EM Channels in milli-seconds.

**Projected deliverables for Year 2 (if applicable):** Model based demonstration of counter measures; prototype development with observer; demonstration of trusted platform using prototype or evaluation board; software for deep learning in matlab.

**Potential Member Company Benefits:** Designers must anticipate every form of attack to prevent access to embedded systems and data. Along with already existing work on AES and TPM (Trusted Platform Module), we believe that this approach will provide an added level of security for trusted platform design.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/19
### Project Summary

**Title:** Causal inferencing for building trust in platform designs  

**Date:** 9/1/17  

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)  

**Tracking No.:** 2A3  

**Project Leader(s):** Shobha Vasudevan  

**Phone(s):** (217)333-8164  

**E-mail(s):** shobhav@illinois.edu  

**Proposed Budget:** $50,000  

**Type:** (New/Continuing/Follow-up) New  

**Other Faculty Collaborator(s):** NA  

**Project Description:** Owing to overseas manufacturing of hardware, IP reuse in SoCs, long and involved supply chains and widespread use of programmable devices, the threat of attacks on platforms has increased manifold in the past few years. This is an important and urgent societal problem that needs long term, sustainable, robust solutions. The solution must respect the constraints of cost and performance, while being fine grained enough to analyze systems with heterogeneous components like processor chips, analog and mixed signal chips, I/O, memories etc. We plan to take a three pronged, cross-layer approach towards making platforms trustworthy.  

1. **Cross layer causality inferencing to analyze threats to design:** By repurposing components of GoldMine, we will be able to analyze the simulation data from the register transfer level (RTL) design to learn patterns of normal behavior. We will use simulation test benches used for verification that are meant to capture various corner case scenarios. We will also use application level “typical” workloads to learn typical behavior of the platform hardware. GoldMine ranks the properties by optimizing how much coverage of the design each property has, and how succinct it is. The top ranked properties will have high behavioral coverage of the design and can be synthesized on the hardware as monitors/assertions. So far, we have generated only hardware assertions in GoldMine. We propose to investigate a hybrid solution, where properties generated from workload applications can operate at the software application level, while some critical system level hardware properties generated from RTL can be synthesized into hardware.  

2. **Diagnosis of intrusion by efficient coverage analysis:** Using our technology for hardware design coverage analysis (Best paper award, DAC 2014), we can compute the design coverage of a property/assertion very efficiently. Given an abnormal/unexpected behavioral pattern from part (1) that violates a GoldMine property, we can map it back to the design and identify the possible culprit IP that was tampered with. We can map the property to the RTL design it covers with our current tools. We propose to research methods to similarly analyze the transaction level for coverage by the application level assertions.  

3. **Ongoing data analysis and updating during lifetime of operation:** We plan to keep the analysis alive during the operational lifetime of the platform. Applications and transactions that are hitherto unseen, will be recorded as new data, and application level monitors updated regularly.

**Progress to Date (if applicable):** Our research software for design verification, GoldMine, can automatically generate invariant properties or assertions, for verifying digital hardware. GoldMine (IEEE TCAD 2013, DATE 2010, DATE 2011, IEEE TCAD 2012, ICCAD 2013, JETTA 2013, GLSVLSI 2013, VLSI Design 2014, DAC 2014; Best paper award at DAC 2014, Best paper award VLSI Design 2014, NSF CAREER award) automates a ubiquitous process that is manual in contemporary hardware industry. GoldMine had practical impact- several EDA and semiconductor companies have licensed GoldMine from UIUC. Since 2013, GoldMine has been available on the web (https://goldmine.csl.illinois.edu) for research and academic purposes. The intellectual insight from GoldMine is that while statistical learning methods rely on correlation based inferencing, causal inferencing is much more difficult and needs external information. GoldMine provides a general framework for deciphering causal relations from data.

**Experimental plan (current year only):** We plan to use the SoC platform that includes OpenSpare T2, a publically available design at RTL and system level transactions. This will be our experimental testbed.

**Related work elsewhere and how this project differs:** We are not aware of any other work that uses a combination of machine learning and static design analysis to infer causality in intrusions.

**Proposed milestones for the current year:** Technique to generate application level properties using GoldMine, technique for combining application and RTL properties for accurate tamper detection and vulnerability prediction

**Proposed deliverables for the current year:** Algorithms/methods to generate application level properties using GoldMine; algorithms to combine RTL and application level properties to detect platform intrusions and predict threats

**Projected deliverables for Year 2 (if applicable):** Algorithms to map violated properties back to transactions that caused them in the application level

**Potential Member Company Benefits:** Novel and effective methods to analyze large and complex designs, detect and diagnose threats, ability to predict and protect vulnerable parts of the design, better comprehension of metrics for trust during design of trustworthy platforms.

**Estimated Start Date:** 1/1/18  

**Estimated Project Completion Date:** 12/31/19
Project Synopsis

**Title:** Machine Learning to predict successful FPGA compilation strategy  
**Date:** 9/1/2017

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)

**Tracking No.:** 2A4  
**Project Leader(s):** Sung Kyu Lim (Georgia Tech)

**Phone(s):** (404) 894-0373  
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**Proposed Budget:** $50,000  
**Type:** (New/Continuing/Follow-up) New

**Other Faculty Collaborator(s):** none

**Project Description:** The goal of our project is to build machine learning (ML) models that produce FPGA compilation recipes that show high success rate and fast compilation time. We assume the following are given as the inputs: (1) RTL and its timing constraint, (2) target FPGA device, (3) FPGA compilation toolset (synthesizer, mapper, placer, router), and (4) compilation recipe (optimization goal, effort level, logic restructuring, random number seed, etc.). Our ML model predicts whether the given recipe leads to compilation success (= RTL fits to the FPGA and its timing goals are met). The model also predicts compilation time. For a given set of recipes under consideration, we use this model to select successful ones and order them based on their predicted compilation time. Because ML-based prediction is quick, we can afford to examine many candidate recipes and choose the best one.

The input to our ML model includes circuit structure-related parameters such as the number of LUTs, FFs, global signals, IOs, net-size distribution, etc. Using these inputs, our ML will predict compilation success rate and runtime. Our special focus will be on the impact of local congestion on compilation failure. We seek toolset parameters and recipes that effectively avoid local congestion and thus improve success rate and time. We believe that congestion can be considered during all major steps of FPGA compilation. During synthesis, we can choose the options that will minimize the number of nets and pins. During mapping, the connections among different logic elements can be minimized. Placement can be guided to minimize local congestion, while routing is the actual step that decides which routing switches to use and thus a more direct impact on routability. However, congestion avoidance may come at the cost of runtime, timing, and power degradation. Our goal is to seek recipes (and potentially improvement on the compilation engines themselves) that strike a balance between congestion, compilation time, and other key metrics.

We will also build models for silicon interposer-based multi-FPGA systems, where FPGA partitioning becomes a key step in deciding the number of IOs required, demand for interposer interconnects, and ultimately the overall compilation success. FPGA partitioning is performed under a strict pin constraint, which is non-trivial to satisfy. In addition, depending on how partitioning is done, on-interposer routing demand may exceed supply. Our goal is to seek related ML-model parameters and recipes that help alleviate burdens imposed on partitioning.

**Progress to Date (if applicable):** none

**Experimental plan (current year only):** We will write codes to access FPGA mapping database, extract key parameters that affect compilation success and runtime, build and train ML models, and process and optimize recipes.

**Related work elsewhere and how this project differs:** Researchers from Tianjin University used ML to optimize FPGA architecture parameters, while Argonne National Lab developed an ML-based tool for FPGA timing and power closure. ML tools from Plunify are producing FPGA compilation recipes for timing closure, and University of Guelph specifically targeted FPGA placement as the key enabler for ML-prediction. However, none of these work address the impact of congestion nor target multi-FPGA systems.

**Proposed milestones for the current year:** Successful recipe constructions and accurate runtime prediction for single and multiple FPGA systems.

**Proposed deliverables for the current year:** Our ML models, scripts, codes, and additional compilation database built in our lab

**Projected deliverables for Year 2 (if applicable):** Our year 2 plan will target ML models and toolsets that help fix/enhance the original RTL codes to improve compilation success and runtime.

**Potential Member Company Benefits:** Our tool will help Synopsys strengthen their FPGA compilation toolset. In addition, FPGA designers in other member companies will save time searching for good recipes.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/19
### Project Summary
**Title:** Applying Machine Learning to FPGA Design  
**Date:** 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)  
**Tracking No.:** 2A5  
**Project Leader(s):** Franzon, Davis (NCSU)  
**Phone(s):** (919) 515-7351  
**E-mail(s):** {wdavis, paulf}@ncsu.edu  
**Proposed Budget:** $53,926  
**Type:** (New/Continuing/Follow-up) Follow-up  
**Other Faculty Collaborator(s):** Baron (NCSU)

### Project Description
In 2017, we proposed a one year project to investigate automating back end flows for ASICs. After being recommend by the IAB, we were asked to break this into three projects (1) back end flows for ASICs; (2) FPGA flows, and (3) CNN for DRC investigation. This proposal is a continuation of the work done in sub-task (2) and also addresses the project in the RFP entitled “Machine learning based prediction of FPGA compilation strategy success.”

In this project, we have the following major objectives (1) determine how to set up a synthesis and physical design flow to meet specific goals for a specific design, (2) determine how to classify designs so that the flow does not have to be run on a per-design basis but instead the tool set up determined by its characterization; (3) determine what the trade-offs are for a design between this setup and the design goals, and between the design goals themselves in the context of a design, and (4) determine design characteristics (based on the classification in objective (2)) that makes it easiest to meet design goals.  
Surrogate modeling will be used to capture the key relationships in a global fashion. The outcome of this step will satisfy both objectives for a specific design. A range of classification techniques will be investigated to determine the best methodology and choice of design characteristics can be used to classify designs so that these objectives can be met for a specific design without having to run that design through the tool flow.  
Possible design characteristics include special resource usage; net/gate ratio, net/flop, and net/adder ratio by region; control fan-in; distribution of fan-in and fan-out. A key objective would be to work out the suitability of various classification vectors. The surrogate modeling flow will be run on a range of designs from our own design library as well as ones provided by CAEML members. By using a range of designs, we can best achieve the classification and design characteristics goals.

### Progress to Date (if applicable)
Though not a renewal, a trial investigation found that we could produce a surrogate model with sufficient accuracy for both Xilinx and Altera flows. The production of these models has been automated.

### Experimental plan (current year only)  
We will start by producing surrogate models for a range of designs, both those sourced at NCSU and those obtained by from CAEML member companies. These models will be used to determine that setup automation and tradeoff automation can be easily achieved for a specific design. Then we will start evaluating possible classification techniques.

### Related work elsewhere and how this project differs
The authors of [1] have partially achieved the goal of how to classify designs according to the placement tool for which they are best suited, focusing primarily on academic tools. They have also shown that that certain routing characteristics can be predicted. Our project will perform the additional work needed to meet specific design goals. In addition, our project will use commercial tools primarily and will consider synthesis all the way through to routing.


### Proposed milestones for the current year
(1) establish the viability of using surrogate modeling to guide tool setup for a specific design and specific design goals, including understanding the impact on tradeoffs; and (2) an understanding of how to classify designs so that this goal can be achieved for a class of designs, not just individually characterized ones.

### Proposed deliverables for the current year
Reports on above. Code and data.

### Projected deliverables for Year 2 (if applicable)
Ability to setup the tools to achieve specific objectives for a design, without the need to characterize that design first.

### Potential Member Company Benefits
Improved design convergence for FPGA designs.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/19
<table>
<thead>
<tr>
<th><strong>Project Summary</strong></th>
<th><strong>Title:</strong> Causal Inference for Early Detection of Hardware Failure</th>
<th><strong>Date:</strong> 9/1/17</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Center:</strong></td>
<td>Center for Advanced Electronics through Machine Learning (CAEML)</td>
<td></td>
</tr>
<tr>
<td><strong>Tracking No.:</strong></td>
<td>2A6</td>
<td><strong>Project Leader(s):</strong> N. Kiyavash, M. Raginsky and E. Rosenbaum (all UIUC)</td>
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<td><strong>Proposed Budget:</strong></td>
<td>$41k</td>
<td><strong>Type:</strong> (New/Continuing/Follow-up) New</td>
</tr>
</tbody>
</table>

**Other Faculty Collaborator(s):**

**Project Description:** A causal inference framework for predicting hardware failures will be developed. The framework will utilize expert knowledge of physics-of-failure and sensor data from the field; sensors monitor performance metrics, environmental conditions, error rate, etc. The methodology will be developed in the context of hard disk drive (HDD) failure prediction since large amounts of sensor and failure data are publically available (from BackBlaze and Baidu storage arrays). HDD “SMART” data include the number of power cycles, number of uncorrected reads, reallocated sector count, temperature, and many other indicators. Our methodology will use the time series data collected through the SMART as well as physical covariates (e.g., temperature) pertaining to a device and to train the predictor. Furthermore, we plan to develop a “causal transfer learning” paradigm that allows us to extend our learning from one device (i.e., one model HDD) to other similar devices. Such a data-driven modeling methodology is ideally suited to capture differences between available device models while avoiding incorrect assumptions about the underlying statistical distributions.

**Progress to Date (if applicable):** N. Kiyavash has developed an information-theoretic framework for causal inference from time series data using both parametric and non-parametric models.

**Experimental plan (current year only):** Evaluate causal inference predictive frameworks using SMART data and HDD failure statistics. Two types of models will be considered for modeling time series SMART data. (1) Non-parametric models for which causal relationships are quantified information theoretically (e.g., using directed information measure). (2) When suitable, parametric models such as autoregressive models or mutually exciting point processes to capture both continuous and discrete events. While parametric models rely on stronger assumptions, they result in reduced sample and computational complexity of the causal inference task. The team will test both types of modeling frameworks to evaluate their suitability for prediction and transfer learning tasks for failure prediction.

**Related work elsewhere and how this project differs:** HDD failure prediction from SMART data has been attempted by several organizations, including UCSD (Murray 2005), Google (Pinheiro 2007), and Nankai-Baidu Joint Lab (Li 2017). Recently, IC field-use data was collected by telemetry and used for knowledge-based qualification of microprocessors (Intel, Kwasnick 2017) and motor drive circuits (Google, Kale 2017). Furthermore, many research groups have worked on benchmarking the life expectancy of their products (or systems) under expected service loads and environmental conditions. Most research in both domains uses simple correlation type metrics or side information about the physics of the system in the form of Bayesian analysis. The longitudinal causal inference techniques advocated here are a major departure from such approaches and allow for principled ways of omitting redundant covariates or features that might be correlated with the failure but do not help in the prediction task.

**Proposed milestones for the current year:** (1) Use domain-specific knowledge to develop statistical models for causal inference. (2) Identify dataset requirements and

**Proposed deliverables for the current year:** (1) Basic demo of a software implementation. (2) Theoretical analysis of algorithm complexity/performance. (3) Technical report to center members.

**Projected deliverables for Year 2 (if applicable):** (1) Large-scale software implementation and validation. (2) Report on cost-benefit analysis and comparison of non-parametric and parametric models.

**Potential Member Company Benefits:** Early detection of component failure may revolutionize system design, e.g. by allowing one to reduce redundancy or lengthen the system lifetime specification. Component failure is of concern on both a micro scale (trillions of Flash memory cells in a solid-state drive) and a large scale (thousands of HDD in a storage array).

**Estimated Start Date:** 1/1/18  **Estimated Project Completion Date:** 12/31/18
Title: Applying Machine Learning to Back End IC Design

Date: 9/17

Center: Center for Advanced Electronics through Machine Learning (CAEML)

Tracking No.: 2A7

Project Leader(s): Davis, Franzon (NCSU)

Phone(s): (919) 515-7351

E-mail(s): {wdavis, paulf}@ncsu.edu

Proposed Budget: $53,925

Type: (New / Continuing / Follow-up) Follow-up

Other Faculty Collaborator(s): Baron (NCSU)

Project Description: In 2017, we proposed a one year project to investigate automating back end flows for ASICs. After being recommend by the IAB, we were asked to break this into three projects (1) back end flows; (2) FPGA flows, and (3) CNN for DRC investigation.

In this project, we will have two major objectives (1) how to set up a synthesis and physical design flow to meet specific goals, and (2) what the trade-offs are for a design between this setup and the design goals. The first goal towards achieving these objectives will be to determine how to set up the tools for a specific design for specific goals. Both the Cadence and Synopsys backend tools have many options that have a strong impact on the achievable speed, resource allocation and compile time. Surrogate modeling will be used to capture these relationships in a global fashion. The outcome of this step will satisfy both objectives for a specific design. The second goal would be to determine how to achieve this mapping for a variety of designs. Classification techniques will be used to classify designs so that these objectives can be met for a specific design without having to run that design through the tool flow. Instead the design would be run through the classifier and the possible classifications will be used to determine the setup and tradeoffs for that design. Possible classification vectors include net/gate ratio by region, net-span distribution, timing criticality coming out of synthesis, slack distribution, etc. A key objective would be to work out the suitability of various classification vectors.

Past work focused on the complete flow including placement and routing. This work will include details on power and clock insertion.

Progress to Date (if applicable): Though not a renewal, a trial investigation found that we could produce a surrogate model with sufficient accuracy for Cadence flows. The production of these models has been automated.

Experimental plan (current year only): We will start by producing surrogate models for a range of designs, both those sourced at NCSU and those obtained by from CAEML member companies. These models will be used to determine that setup automation and tradeoff automation can be easily achieved for a specific design. Then we will start evaluating possible classification vectors that can be used to characterize designs. Vectors will be evaluated for their correlation to design objectives and tool set up alternatives. We will investigate detailed flows for automated power rail and clock insertion.

Related work elsewhere and how this project differs: There is no similar work we are aware of.

Proposed milestones for the current year: (1) establish the viability of using surrogate modeling to guide tool setup for a specific design and specific design goals, including understanding the impact on tradeoffs; (2) establish the viability of using surrogate models for power rail and clock insertion, and (d) an understanding of how to classify designs so that this goal can be achieved for a class of designs, not just individually characterized ones.

Proposed deliverables for the current year: Reports on above.

Projected deliverables for Year 2 (if applicable): Ability to setup the tools to achieve specific objectives for a design, without the need to characterize that design first.

Potential Member Company Benefits: Improved design convergence for ASIC back end flows.

Estimated Start Date: 1/1/18

Estimated Project Completion Date: 12/31/19
**Project Summary**

**Title:** Applying Machine Learning to Design Rule Checking  
**Date:** 9/1/17

**Center:** Center for Advanced Electronics through Machine Learning (CAEML)  
**Tracking No.:** 2A8  
**Project Leader(s):** Franzon, Davis (NCSU)  
**Phone(s):** (919) 515-7351  
**E-mail(s):** {paulf, wdavis}@ncsu.edu  
**Proposed Budget:** $53,926  
**Type:** (New / Continuing / Follow-up) Follow-up  
**Other Faculty Collaborator(s):** Baron (NCSU)

**Project Description:**

In 2017, we proposed a one year project to investigate automating back end flows for ASICs. After being recommend by the IAB, we were asked to break this into three projects (1) back end flows; (2) FPGA flows, and (3) CNN for DRC investigation. This project is a request to extend the third project.

In this, the “full version” of the project, we propose two directions. The first is to complete the demonstration using additional rules from the NCSU 15 nm PDK full rule set. The second is to start investigating possible ways to tie this project to the rule derivation.

To completely demonstrate a more complete rule set, the methodology in the project would have to be extended to handle larger rule spans than we have now and to more conditional rules. In addition, we need to move to conducting feature extraction before fitting a ML model. Possible techniques include using SKILL, a support vector machine or an edge extraction algorithm. We also plan to investigate a range of ML models to determine which provides the best fitting accuracy. While the NCSU 15 nm PDK has only a small number of rules, showing it working on several of those rules, especially ones that interact between multiple layers, would give greater confidence of it being extendible to a full industry rule set without having to deal with proprietary data.

The second objective is to look at machine learning to fix the connection between the fab the design rule paradigm. We will investigate replacing the design rule paradigm with a neural network. A hypothetical yield monitor would be designed and populated with hypothetical failures. A neural network will be fitted to that model and then that network applied to a design. This will lead to a basic demonstration of the potential for this paradigm.

**Progress to Date (if applicable):**

Though not a renewal, a trial investigation was conducted to demonstrate the feasibility of using convolutional neural networks to replace one rule. A range of SRAM designs were obtained from the VLSI class. These were modified to produce 5,000 alternative designs. These were run through the 15 nm PDK to produce labelled data for one Metal 1 rule. That data was used to fit a CNN. Final results are being evaluated as the proposal is being written.

**Experimental plan (current year only):**

We will repeat the experiment done in the first year but with multiple rules, including inter-layer ones, and more sophisticated modeling techniques. Explicitly we will focus on doing feature extraction first so that the networks don’t have to deal with the large amount of data exposed by treating the layouts as pixelated images. We will also investigate multiple different models not just the “off-the-shelf” one used in the preliminary experiment. Fortunately, we now have in place all the methodology to produce 1000s of labeled designs based on a class SRAM design.

**Related work elsewhere and how this project differs:**

We are not aware of any directly related work.

**Proposed milestones for the current year:**

(1) Establish the viability of building ML models to cover a more complete rule set; (2) measure the false positive and false negative rates with this rule set.

**Proposed deliverables for the current year:**

Reports on above.

**Projected deliverables for Year 2 (if applicable):**

Demonstrate the feasibility of using machine learnt networks as a direct replacement for the concept of design rules.

**Potential Member Company Benefits:**

Better, easier DRC management, quicker DRC runs, and a direct connection between fabrication and design rule checking.

**Estimated Start Date:** 1/1/18  
**Estimated Project Completion Date:** 12/31/19
## MEETING ATTENDEES

<table>
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<tr>
<th>Name</th>
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