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Metal/semiconductor interactions

Allen, Leslie Henry, Ph.D.

Cornell University, 1990

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METAL/SEMICONDUCTOR INTERACTIONS

A Dissertation

Presented to the Faculty of the Graduate School

of Cornell University

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

by

Leslie Henry Allen

May 1990

BIOGRAPHICAL SKETCH

Leslie Henry Allen was born on February 2, 1952 in of Dickinson, North Dakota, a farming community in the great plains region. He attended St. Patricks elementary school and Trinity High School where he enjoyed trombone and science fairs. In 1975 he graduated from the University of North Dakota in mathematics. For the following year, he adventured about Mexico where he met Joy Okoniewski, his future wife. After obtaining a masters degree in physics from Clarkson University in Potsdam, NY (1979), he worked for the next four years at SES (a subsidary of Shell) Newark, DE developing the CuSCdS solar cell. During this period, the first part of the family was born, Nathan (December, 1981) and Arlie (March, 1983). When SES was liquidated, he continued his career in photovoltaics at McDonnell Douglas, St. Louis, MO developing the HgCdTe infrared detector. He entered Cornell University in August, 1985 and completed the Ph. D. program in the Materials Science department in May,1990. His family's third child Lydia, was born in September, 1989.

Dedicated to

Mom and Dad, who encouraged dreams,

and to Joy, who encourages their fulfillment

ACKOWLEDGMENTS

I begin by thanking my immediate family, for allowing me the opportunity to return to graduate school and pursue my career in science. Joy became our breadwinner and resident psychologist throughout this period.

Thanks to my mentor, Professor Jim Mayer, who gave me the opportunity to practice this art of science within an environment rich in excitement, encouragement and common sense. His idea that things should be explained in simple ways, is a testament to his understanding of how real learning takes place.

I would like to thank Professor Mike Thompson for his help with computers especially for his invention of GENPLOT, and Professor Lester Eastman for our discussion about ohmic contacts to GaAs. The abundant resources within Cornell were easy to tap, thanks to the Ray Coles, John Hunt, Margret Craft (microscopy group), Margret Rich and Maura Weathers (x-ray group), Larry Doolittle, Nick Szabo, Peter Revez, Peter Borgeson and D. Lilienfeld (RBS), Jane Jorgensen (artistry) , Steve Springer, Marcia Kelley (photography), Noreen Ocello (system coordinator), Marlene Rietz, Carrol Armstrong, Cora Banks, Bob Terry, Helen West, Josie Lovejoy, Bill Van Duzer, Seymor Maltese (support), Gerhart Schmidt, Ron Kemp (TOL, Clark), Bob Soave, Lynn Rathbun, George Porkolab, Greg Galvin, Harold Craighead (NNF), David Stanasolovitch, Dave Thomas, Susan Arney (Professor Wong's processing group).

Through Professor Mayer I had wonderful interactions with people

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Many useful discussions and collaborative efforts were engaged with other members of our group, including Terry Alford, Bart Blanplain, Betsy Fleischer, Qi-Zhong Hong, Hyodo Tomo, Hiro Kuwano, Jian Li,Randy Phillips, Rick Purser, Steve Russel, Shi-Qing Wang, Anthony Yu, Mark Zaleski, Lian Sun Hung, Long Ru Zheng.

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Part I

Au/polysilicon reactions and the *in-situ* sheet-resistance measurement

Chapter 1

Introduction

1.1 Introduction

This thesis is organized into two parts. Part I investigates the thermodynamics and kinetics of the reaction between Au/polysilicon, and describes a useful technique for studying thin film reactions: the *in-situ* sheet resistance measurement. In Part II, the common theme for discussion is interface problems, such as ohmic contacts to GaAs and the growth of W on Al. The introduction in chapter 7 details the objectives of the studies in Part II.

The first topic discussed in Part I (chapter 2) focuses on the *in-situ* sheet resistance measurement technique. First, a description of the physical apparatus for the measurements is given. Following this, the methodology and uses of the system are outlined, including examples of qualitative and quantitative experiments.

The remaining chapters of Part I are concerned with the different aspects of the reaction between Au/polysilicon. Chapter 3 discusses the overall morphological process of Au and silicon redistribution during the anneal, using XRD and the SEM to identify the Si crystals. Chapter 4 describes the kinetics of the reaction by using the results of in-situ resistance as well as SEM measurements. Engineered crystal growth is the topic of chapter 5, this chapter shows the results of a few experiments which were prompted by the results of the two previous chapters. Finally, in chapter 6, emphasis is

given exclusively to the redistribution of the Au during the Au/polysilicon reaction. The importance points of this chapter are related to real reliability problems associated with metal spiking through polysilicon layers. This problem currently has a high profile because of spiking problems of PtSi contacts to polysilicon, where shunting occurs in shallow bipolar emitters.

The work on Au/polysilicon was initially motivated by the desire to understand a the stability of metals on polysilicon. Au was chosen, rather than other metals, for three reasons: Au doesn't easily oxidize, it has a heavier mass as compared with Si making analysis easier, and it reacts with polysilicon at relatively low temperatures.

The Au-Si bulk phase diagram (Fig.1.1), shows two interesting things about the Au/Si system: (1) they are essentially immiscible in the solid phase (they don't like each other), and (2), they form a very deep eutectic at 360°C, several hundred degrees below the each component's melting temperature. The extrapolated values for the concentration of Au in Si at temperatures below the eutectic is on the order of $10^{10}/cm^3$, an immeasurable quantity for most standard techniques (SIMS etc.). The concentration of Si in Au is higher, but still too low to be measured via AES, EDX or RBS analysis. To date, the author has not found value in the literature, for the solubility limits or the diffusion coefficient.

This finishes the introduction chapter. This chapter is somewhat abbreviated due to the format of the thesis, which has an introduction section within each chapter.

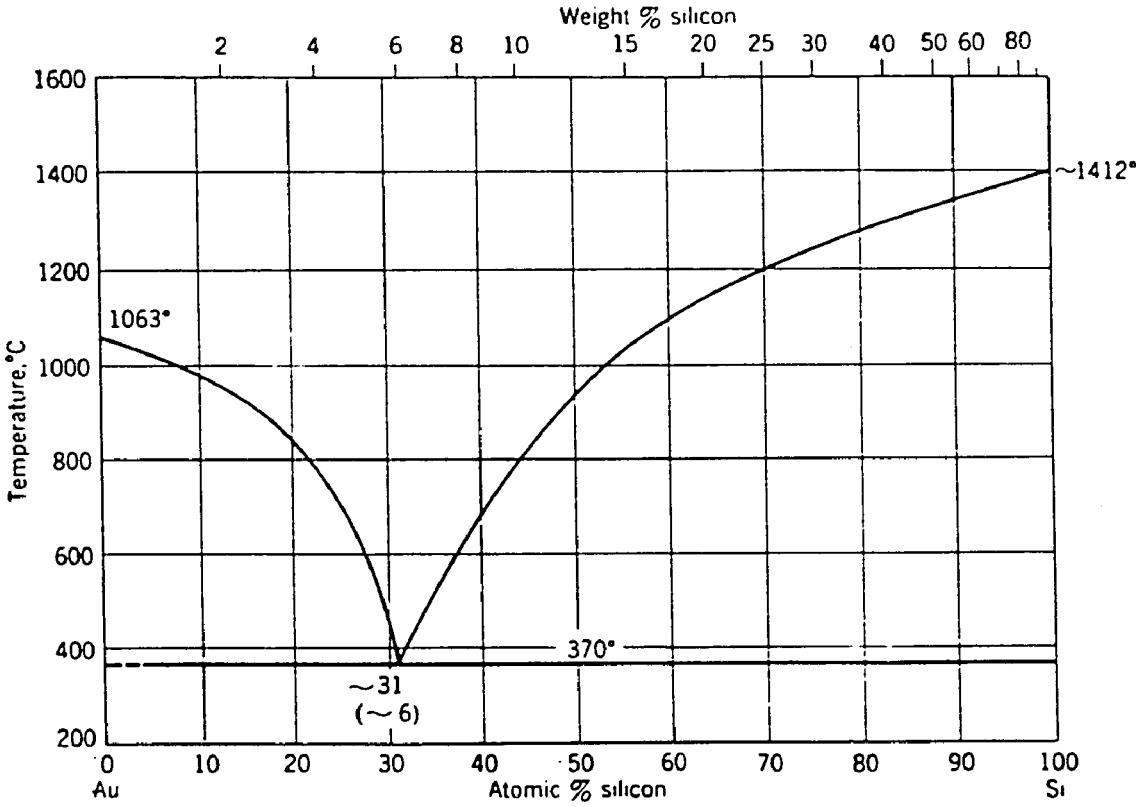

Fig. 1.1 The phase diagram of the Au-Si system.

1.2. References

1. M. Hansen and A. Anderko, Constitution of Binary Alloys, McGraw-Hill, New York, 1958

Chapter 2

The in-situ resistance measurement

2.1 Introduction

Many thin film characterizations tools have been used throughout this work, including RBS, TEM, SEM, XRD and AES. One method which is particularly useful in the study of thin film reaction-kinetics is the *in-situ* sheet resistance measurement. It has been a useful technique for studying the reaction-kinetics of systems many thin-film systems. The first time the author used the *in-situ* resistance method was for the investigation of stoichiometry changes of $Cu_{2-x}S$[1] during thermal annealing in oxidizing and reducing ambient gases. Discussions with Ottaviani[2] and Tu revealed that this method could be used in investigations of phase formation and grain growth in thin-films.

In the following section, a description is given of the physical apparatus which was built for the purpose of monitoring the sheet resistance of samples (*in-situ*) measurements during vacuum furnace anneals. Several experiments will then be described which illustrate the usefulness of the technique. This technique is not exclusive to vacuum furnace or ambient gas anneals but can also be used to monitor reaction kinetics during ion beam mixing. An example of the ion beam *in-situ* resistance measurement will be described in the last section of the chapter.

2.2 *In-situ* sheet resistance apparatus

The *in-situ* resistance measurement apparatus, used for this work, was designed and built by modifying an already existing vacuum furnace system built by E. Colgan[3] . The vacuum furnace is heated by a single-zone resistive heater coil that surrounds a quartz tube that houses the sample. A turbomolecular pump is attached to one end of a five foot quartz tube, the sample exchange port is attached to the other end. This system is capable of maintaining a pressure of 10^{-7}-10^{-8} Torr, as measured by an Varian™ ion gauge that is located on the pump side of the quartz tube. The furnace and sample mounts are capable of anneals up to 950°C.

Samples were mounted onto a mechanical stage having four pressure-contact probes, which is used in obtaining sheet resistance measurements. This four-point probe assembly had the following characteristics:

(1) each probe has adjustable, independent, pressure contacts

(2) the probe tips can be easily interchanged (i.e. W, Mo,Ta etc.)

(3) constant pressure is maintained by a spring (piston) system located outside of heat zone, and

(4) only high temperature material (ceramic,stainless steel) and probe metal is exposed to the heat.

Sample temperature is monitored by a thermocouple (type K - chromel/alumel) mechanically attached to the sample base holder. Kinetics studies during thermal anneals are performed either at constant temperature or at a constant heating rate. However, any temperature algorithm could be programmed, since the furnace temperature was controlled via the computer.

The entire experiment was controlled (see Fig. 2.2) by an AT&T 6300™

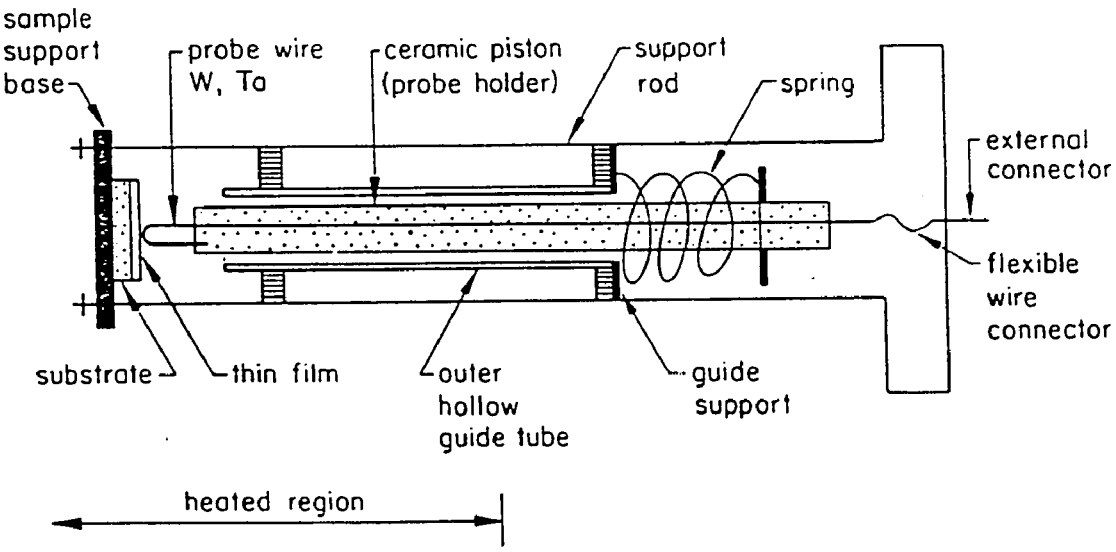

Fig. 2.1 Schematic diagram of in-situ resistance measurement assembly showing 1 of the 4-point probes. Note the spring which provides constant pressure top probe tips is outside of heated region.

personal computer PC expanded with several interface boards. Control of the temperature of the furnace was accomplished via a Eurotherm™ temperature control unit. The analog output/input signals are interfaced to the PC via a Data Translation™ D/A and A/D board. Sample temperature is monitored through an Omega™ digital thermometer/cold-junction, which communicated (digitally) with the PC through the RS232™ serial port.

The resistance measurement are made by applying a given current, via a Keithley™ 200 constant current source, to two adjacent probes of the four probes. On the two remaining probes, the voltage was sensed using a Keithley™ 197 digital multimeter DMM. In order to obtain more accurate resistance values, the data averaged with both polarities of current. Both the current source and the DMM was interfaced to the PC via a National Instrument™ IEEE 488 interface board.

2.3 Examples of *in-situ* sheet resistance measurements

The author has collaborated on a number of projects that employs the *in-situ* sheet resistance measurement. It is the intent here in this section to discuss these projects in terms of methodology, and to demonstrate the potential of the resistance method as a measurement tool.

The first subsection, entitled "Semiquantitative analysis", describes various experiments which use the resistance method to semiquantitatively understand general details of a particular process. In the second subsection entitled "Quantitative analysis using the resistance method ", examples are described where the resistance method is used in a more quantitative mode, the results of which yield specific (kinetic) parameters such as reactions rates and activation energies.

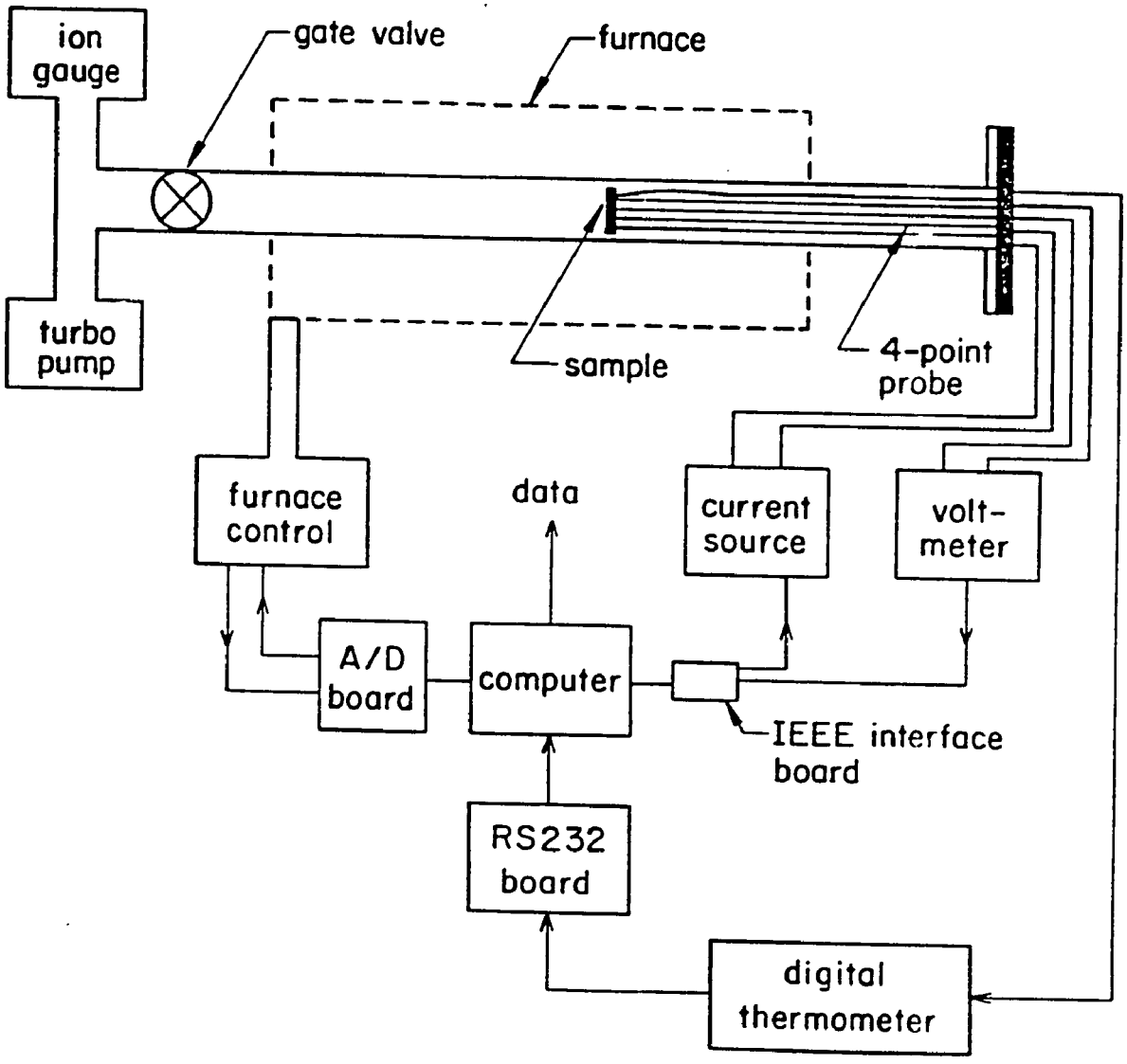

Fig. 2.2 Diagram of in-situ resistance system including furnace (25-1000°C), 4-point probe assembly, thermocouple and data acquisition and control system.

2.3. Semiquantitative analysis

The first example of the semi-qualitative use of the resistance method is the investigation[4] of the amorphization and recrystallization of Al/Pt bilayers during thermal annealing. This system is interesting because the two separate (Al and Pt) layers are initially polycrystalline, but after annealing at low temperatures (≈150°C) the interdiffused, reacted layer is amorphous. The following discussion of the Al/Pt system exemplifies the way, which the resistance method can be used semiquantitatively for general thin film investigations.

Typically, the first experiment of any unknown reaction using the *in-situ* measurement, is done, while annealing the sample at a constant rate (2°C/min). For example, in the case of Al-Pt (Fig.2.3), a sharp increase resistance is observed (factor of ≈15) as the temperature increases to 150°C. This abrupt change in resistance indicates possible abrupt changes in structure and/or composition of the bilayers. After further annealing of the samples, a sharp decrease in the resistance is observed at approximately 250 °C.

In order to relate these changes in resistance to a material property (s), several samples were annealed for intermediate times (A,B,C and D Fig. 2.3 and 2.4.), and then analysed by RBS, TEM and XRD techniques. The increase in resistance at ≈150°C is due to the interdiffusion of the layers, resulting in an intermediate layer, which is shown to be amorphous by XRD and TEM analysis. If the anneal is continued to higher temperatures (points C and D on Fig. 2.3), the resistance abruptly decreases, due to the recrystallization of this amorphous layer, forming polycrystalline Al-Pt compounds.

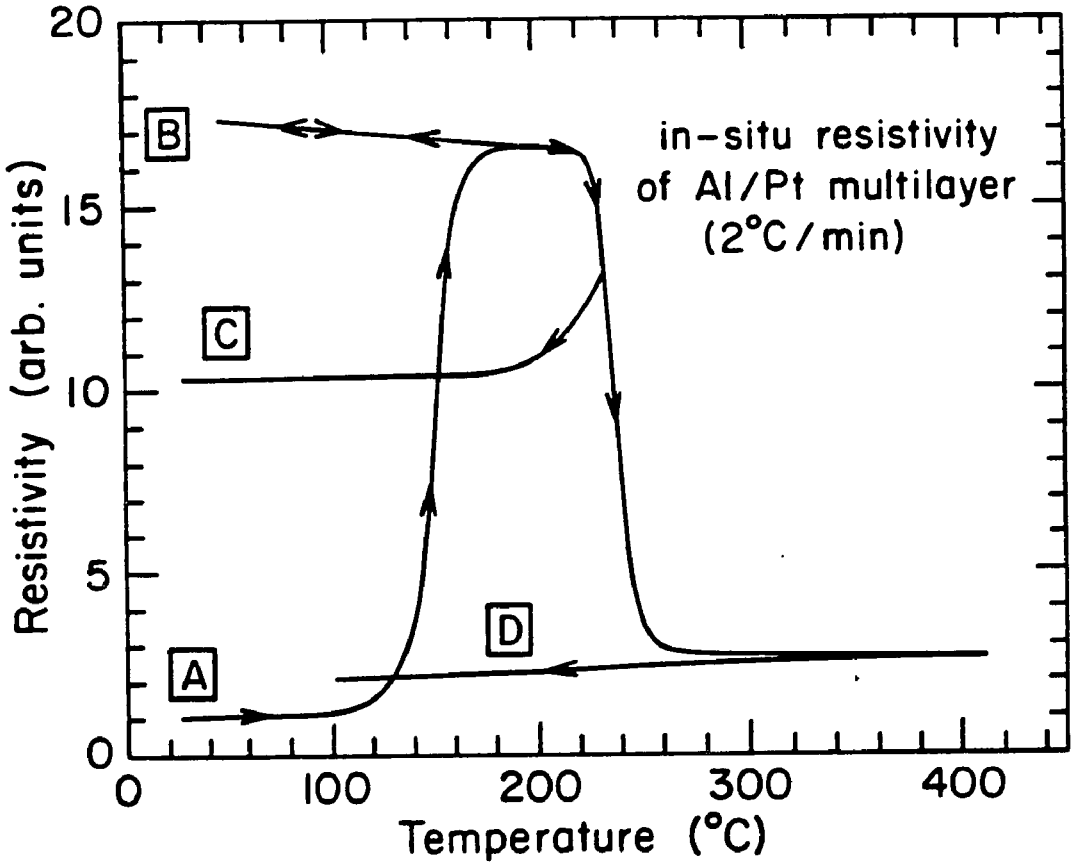

Fig. 2.3 Sheet resistance vs temperature data taken in-situ during constant rate (2°C/min) heating of Al/Pt bilayers. The identified regions of the curve show the sample [A] as deposited, [B] fully amorphized, [C] partially crystallized, and [D] fully crystallized.

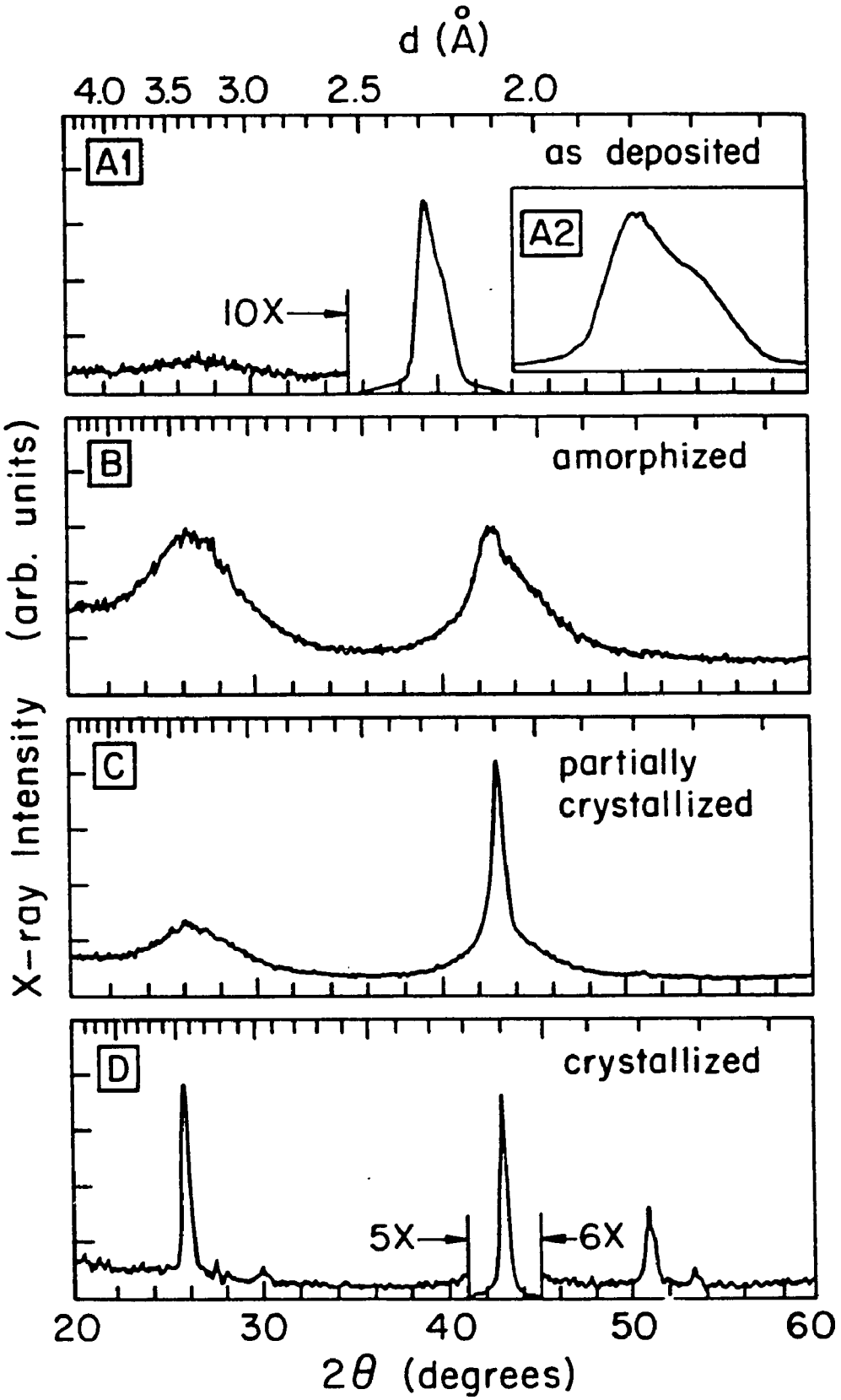

Fig. 2.4 X-ray diffraction data of an Al/Pt sample taken at the different stages during thermal - [A] as deposited, [B] fully amorphized, [C] partially crystallized, and [D] fully crystallized.

The Pt/Al reaction has been further analysed quantitatively by B. Blanpain[5] by performing experiments at constant temperature anneals. From these data, information on the mode (time dependence) of the amorphization and recrystallization processes is obtained[5]. Additional experiments over a range of temperatures yields the activation energy of these processes.

It is useful to digress at this point, and note an important feature of the resistance method; the capability of monitoring a system continuously, as shown in the heat-up and cool-down curves in Fig. 2.3.. This capability provides a qualitative way of checking reversibility of a particular state, and a means by which the temperature-dependent parameters can be separated from the time dependent parameters. Most other measurements (e.g..RBS) performed after the anneal only provide snap-shot analysis of the system after it cools down.

In continuing our general discussion of the resistance method, another investigation is described. This study of compares the stability of Pd_2Si formed on polysilicon with Pd_2Si formed on a SOS (Si On Sapphire). The data in Fig. 2.5 was generated by annealing the samples at a rate of 5°C/min. It is can be deduced from the data, that the Pd_2Si silicide forms at 200°C for both polysilicon and single crystal samples. After annealing to higher temperatures, the silicide layer on the polysilicon becomes unstable (625°C), whereas the silicide layer on the single crystal substrate remains relatively stable until 725°C. The instability is thought to be due to the instability of the polysilicon layer, in the same way as metal/polysilicon system are unstable, which is the main topic in chapters 3 and 4.

There were other investigations using the resistance method during the

course of this thesis work, including experiments designed to test the effectiveness of an amorphous CoW diffusion barrier in the Al/CoW/Si system[7,8]. The reaction of Cu and Si was also evaluated[9].

2.3.2 Quantitative analysis using the resistance method.

As illustrated by the Al-Pt reaction in the previous section, the resistance of a thin film can be a strong indicator of changes in the film, but care must be taken when attempting to relate resistance data to other critical parameters of the reaction. Resistivity of a thin film is a complex parameter, dependent on many factors, for example; grain size, grain boundaries, impurities etc.. To make matters worse, in many cases these properties (grain size, grain boundaries, impurities, etc.) are not uniform; typically, a polycrystalline sample has a wide distribution of grain sizes and the impurities are most likely to be distributed in a nonuniform way. Furthermore, the newly created, reacted layers (with their own set of impurities, grain sizes,etc.) produce a whole new set of unknown characteristics of the system.

Given the uncertainty in the variables which control the resistance, it is somewhat surprising that the method is useful at all. Fortunately, it is the relative changes in resistance which are most important. In most cases, changes in resistance are substantial and can be easily measured The (relative) raw data are usually very precise and reproducible from sample to sample. However, It is the interpretation of these data which gives rise to the difficulties in quantitative analysis.

The core of the problem resides in relating the measured parameter (resistance) to the key parameter of interest. For example, in evaluating

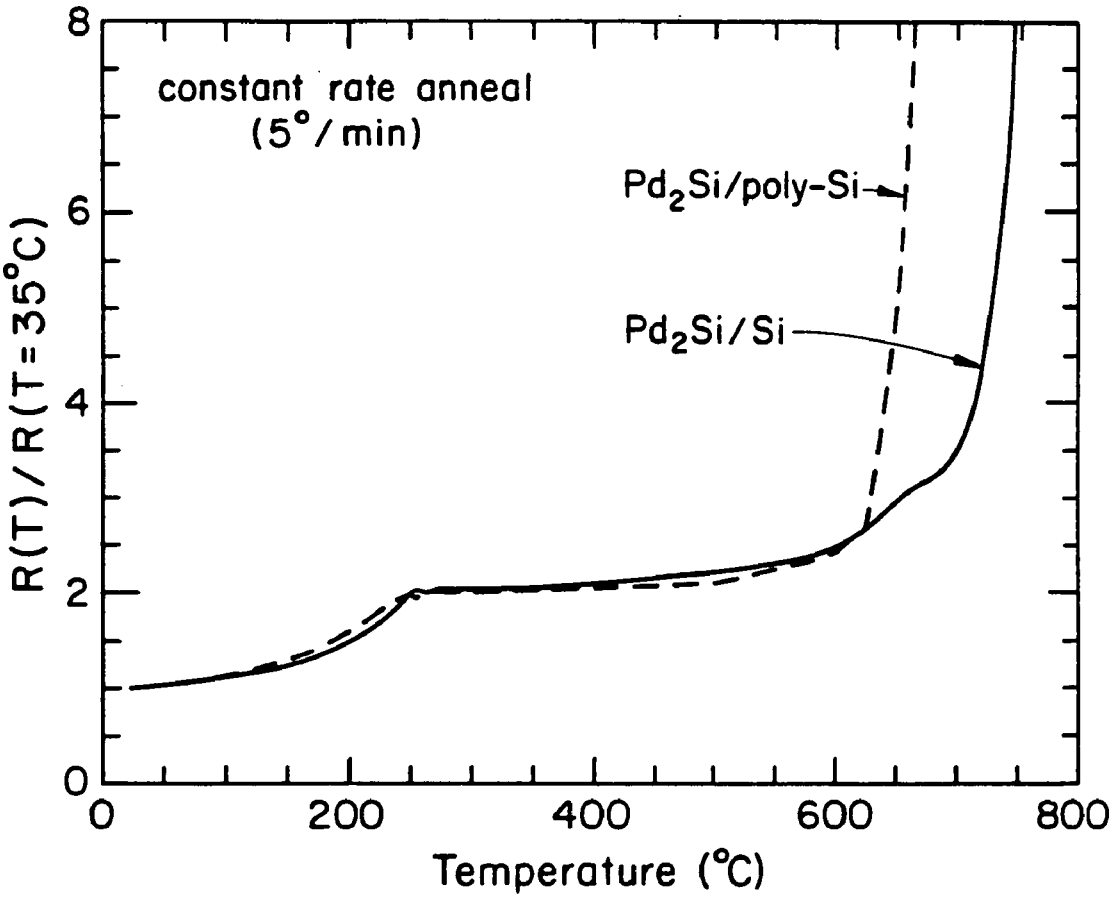

Fig. 2.5 Resistance (in-situ) vs. temperature data during thermal annealing with a temperature increase (5°C/min). A comparison is made between Pd/polysilicon and Pd/crystal-Si shows that the Pd/polysilicon sample is more unstable. Note the silicide reaction ($2Pd + Si = Pd_2Si$) at ≈ 250°C for both samples.

the reaction between bilayers "A" and "B", which produces a new phase "C", we seek an analytical expression relating the resistance to the rate at which "C" is formed. Although, the resistance may change in a straightforward and progressive manner, the resistance data, alone, may have only marginal value. Without specific knowledge of the geometry and mode of reaction of the transformation, the data can lead to ambiguous interpretations. Using the resistance data alone is an invitation to disaster, leading to models, which generate self-consistent nonsense.

Not all is lost though, it is simply necessary to adopt simple, verifiable models which relate the physical parameter of interest (for example the volume of the "C" phase), with the resistivity of the film. Typically, this relationship is established using other independent measurements (i.e. RBS, XRD, etc.), of only a few of the samples from the experiment..

One may ask, that if other methods are needed to "calibrate" the resistance method, why not just use these other methods in evaluating the reaction? The answer lies with the strengths of the resistance measurement: the simplicity of the measurement, the ease of manipulating the data, the sensitivity and precision (+/- 0.1%) of the measurement, and the ability to easily measure the state of the system semi-continuously over a wide range of temperature (20-950°C) and time (1 -10^5 sec) constraints.

2.3.3 Quantitative experiments

Several quantitative studies have been done during the course of this thesis using the resistance method, including the investigation of the reaction between Au and polysilicon, which will be discussed in chapters 3

and 4, but because of its simplicity, we choose reaction between Pt and Si-Ge to demonstrate the applicability of the resistance method to quantitative kinetic studies. This straightforward reaction was first characterized[11] by others (using RBS and XRD), and is similar in many respects to the well known reaction of Pd_2Si silicide. The study[10] shows that the reacted layer (a mixture of Pt_2Si and Pt_2Ge) forms via layer-by-layer growth.

This investigation proceeds as follows, the sheet resistance of the Pt(2000 Å)/Si-Ge sample was monitoring (Fig.2.6) during constant temperature (T≈ 235°C) anneal. Now, since we know that the reaction proceeds layer-by-layer, it is possible to model the reaction in terms of three parallel, layered regions (Pt/Pt_2Si-Pt_2Ge/Si), each layer with their given specific resistivities (ρ_{Pt}, $\rho_{Pt2Si\text{-}Pt2Ge}$ and ρ_{Si}) and thicknesses (d_{Pt}, $d_{Pt2Si\text{-}Pt2Ge}$ and d_{Si}). Assuming that the layers act as parallel resistors the total measured R_T can be expressed as .

$$1/R_T = d_{Pt}/\rho_{Pt} + d_{Pt2Si\text{-}Pt2Ge}/\rho_{Pt2Si\text{-}Pt2Ge} + d_{Si}/\rho_{Si} \qquad (2.1)$$

Since the sheet resistance of the Si substrate (at these temperatures) is much larger than the Pt or Pt_2Si-Pt_2Ge layers, the effects of the substrate are neglected. The extent of the transformation of the reaction $X_R(t)$, which is the fraction of the initial Pt layer consumed during silicide formation, can be quantitatively related to the resistance of the sample by coupling the thickness of the Pt with the thickness of the silicide layer, via the relationship

$$1 - X_R(t) = d_{Pt(t)}/d_{Pt(t=0)} = 1 - d_{Pt2Si\text{-}Pt2Ge(t)}/d_{Pt2Si\text{-}Pt2Ge(t=\infty)} \ , \qquad (2.2)$$

where $d_{Pt(t=0)}$ is the initial Pt thickness and $d_{Pt2Si\text{-}Pt2Ge(t=\infty)}$ is the final Pt_2Si-Pt_2Ge thickness. The transformation factor factor, X_R, can then be explicitly written in terms of the measured quantities,

$$X_{R(t)} = [\,(R_o - R_{(t)}) / (R_o - R_F)\,]\, R_F/R_{(t)} \ , \qquad (2.3)$$

where R_o and R_F are the initial and final values of resistance respectively.

Data from four isothermal anneals are shown in Fig. 2.7a and plotted in

the form of $X_R(t)\ X_R(t)$ vs. t. The reaction has a parabolic time dependence, indicative of a diffusion-limited reaction. This result was confirmed by RBS[10] analysis of several samples, annealed for different times. Assuming that the activation energy E_A for the process can be expressed as

$$X_R(t)\ X_R(t) \propto \exp(-E_A/kT)\ t\,, \tag{2.4}$$

then E_A can be evaluated from the slope $X_R(t)\ X_R(t)/t$. By plotting (Fig.2.7b) the logarithm of the slope vs 1/T(°K) the activation energy E_A = 1.3, which compares well with the value (E_A = 1.2) obtained with the RBS data[10].

It is noted that the results of this study (diffusion limited growth and E_A = 1.3) were the same as those obtained from RBS analysis, yet were obtained with fewer than five 1.0 cm^2 samples, in less than three days, and consumed less than 6 hours of the experimenter's time (given that the initial samples were already made).

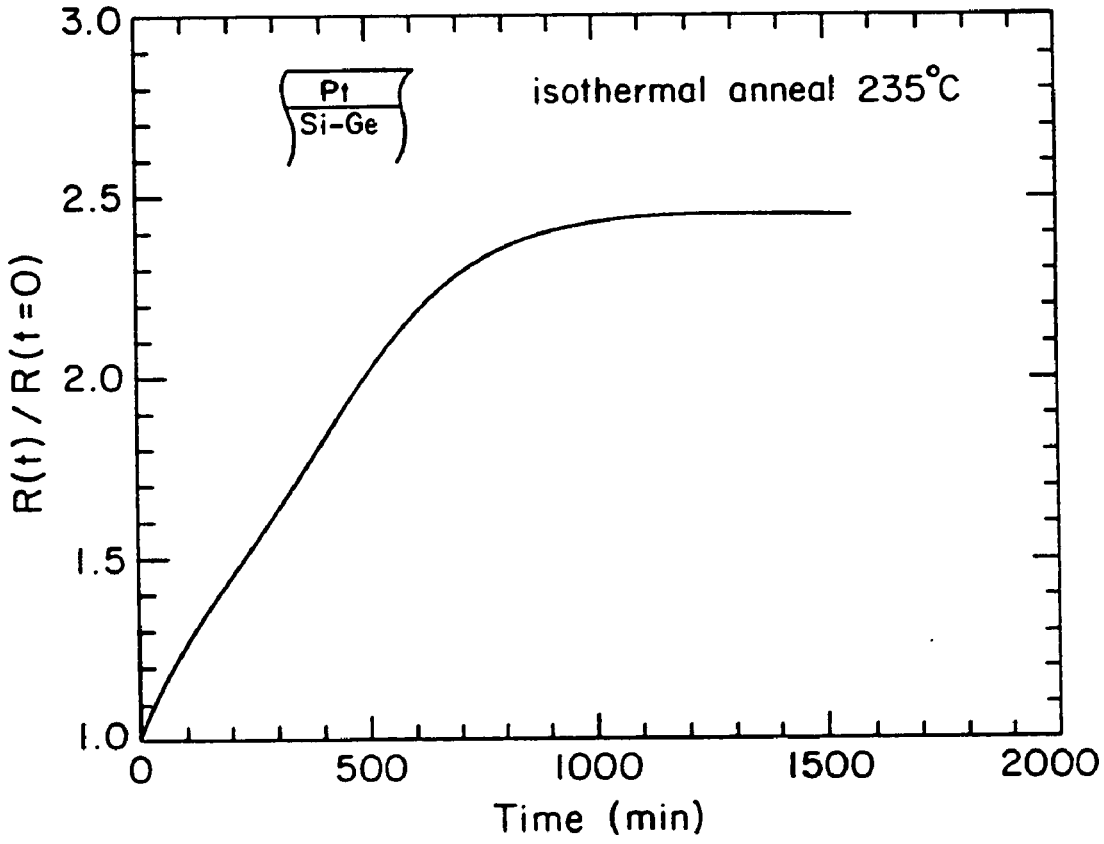

Fig. 2.6 Normalized in-situ resistance vs. temperature data during constant temperature anneal (235°C) of the silicide formation between Pt and Si-Ge.

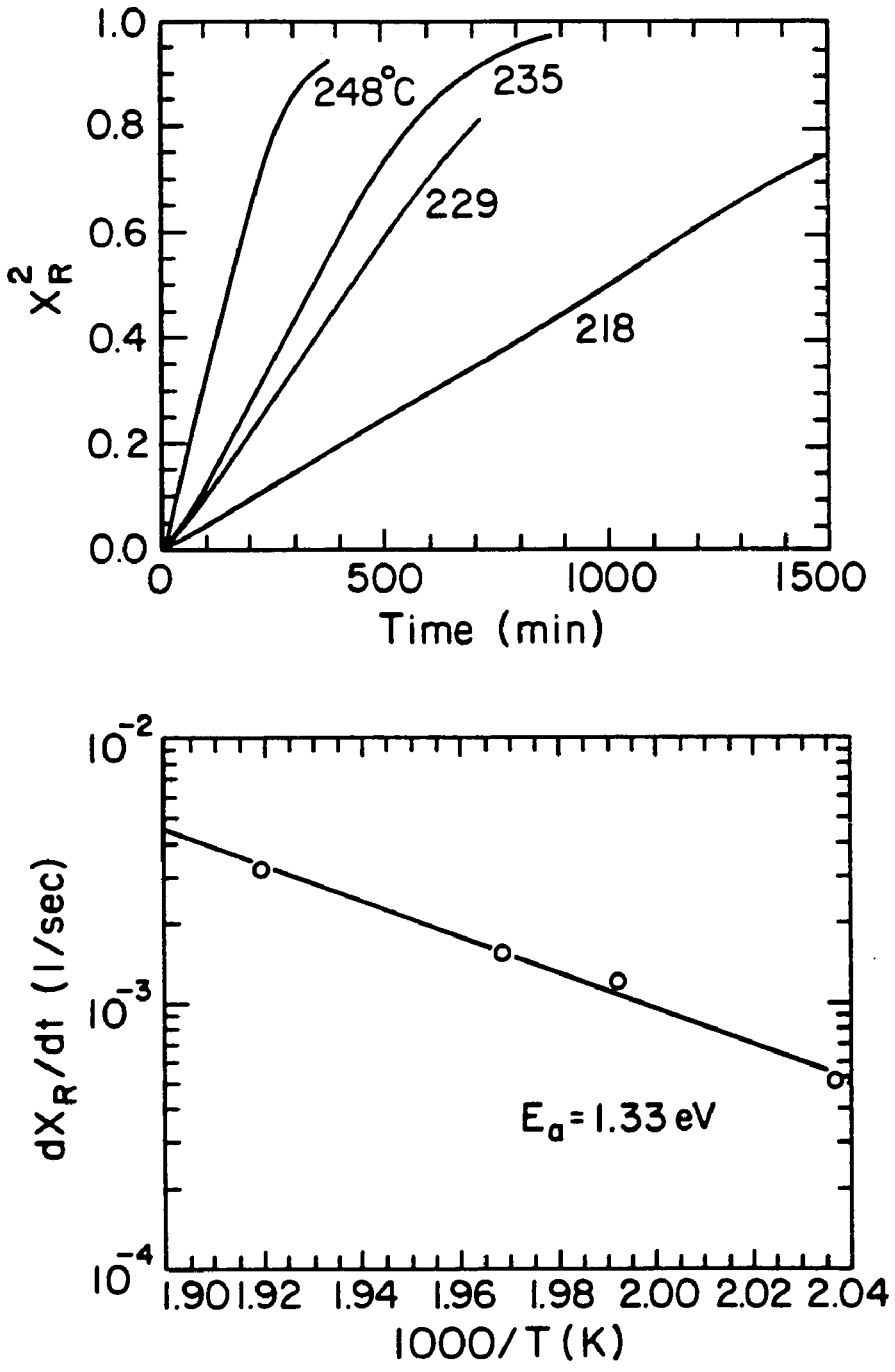

Fig. 2.7 A plot (a) of the square of the (normalized) Pt-Si-Ge thickness X vs anneal time (t) during isothermal anneals at 248, 235, 229 & 218°C. The linear dependence of X^2 vs t indicates a parabolic, diffusion limited reaction process. A plot of the reaction rate vs 1/T yields the associated activation energy $E_a \approx 1.33$ eV.

2.3.4 Evaluation of the stability of Al lines

The final example application for the resistance method, involves the evaluation of the structural stability of Al fine lines (1 μm)[11,12]. (Samples were prepared for the author by Prof. C.Y. Li's group). Al was deposited onto a thermally oxidized Si substrate. Fine lines of the Al were made by standard lift-off techniques. After evaporation, there was only little residual stress within the Al lines, since the processing was done, near equilibrium conditions. The samples were then thermally cycled and there will be stress induced in the Al lines, due to the difference in the thermal expansion coefficient between Al and the substrate. Now, after the samples return to ambient temperature, the lines will be under stress, and eventually voids form, which reduces the stress in the film. The dimensions of these voids are on the order of a μm, thus voids extending the full width of the line, will cause narrow lines to become discontinuous ("opens").

In order to measure the void formation with resistance methods, special samples, containing a digitated set (50 to 100) of parallel grid lines (Al), were fabricated. The lines were connected together at the ends by large pads, which served as probe pads for the four- point probe assembly. Resistance was measured across the pads for extended periods of time at a given temperature. Abrupt, discrete increases in the resistance, as shown in Fig.2.8 were observed. These changes are deduced to be caused by voids being formed in a line, which creates a discontinuity, ("open" line). This discontinuous line will then cease to carry current, thus reducing the number of lines (by one), which contribute to the parallel set of resistors.

By using the resistance method, it is conceptually possible to monitor the kinetics of individual void formation. The plot in Fig. 8a shows the

change in resistance at the time of a discrete event (data acquisition rate ≈ 1/2 min). Faster data acquisition could give a more continuous picture of the individual void formation.

One particular concern, associated with this measurement, is the current density, it must remain low throughout the measurement, in order to eliminate the effects of electromigration[13]. Since the resistance of the structures are inherently low, due to the high conductivity of Al, and because the lines are thick on the order of 1 μm, the voltage signal due to the applied (small) current across the sample is exceedingly small. This may produce signal to noise problems. To increase the signal to noise ratio a Stanford™ Lockin-Amplifier has been used.

2.4 *In-situ* resistance measurement during ion beam mixing

In-stu resistance measurements have also been applied in the kinetic study of reactions during ion beam irradiation (ion beam mixing). A special probe assembly shown in Fig.2.9 was fabricated on the suggestion of J. Li[14], and it serves the same function as the contact probe assembly built for the vacuum furnace system. Typical results of the *in-situ* resistance technique are shown in Fig.2.10 for the Au/polysilicon reaction during ion beam mixing.

The *in-stu* resistance measurements during ion beam mixing has been used successfully for several other experiments including oxygen implantation of high Tc (YBCO) material[15](at liquid nitrogen temperature), and ion beam mixing[9] of thin films of Cu on Si substrates.

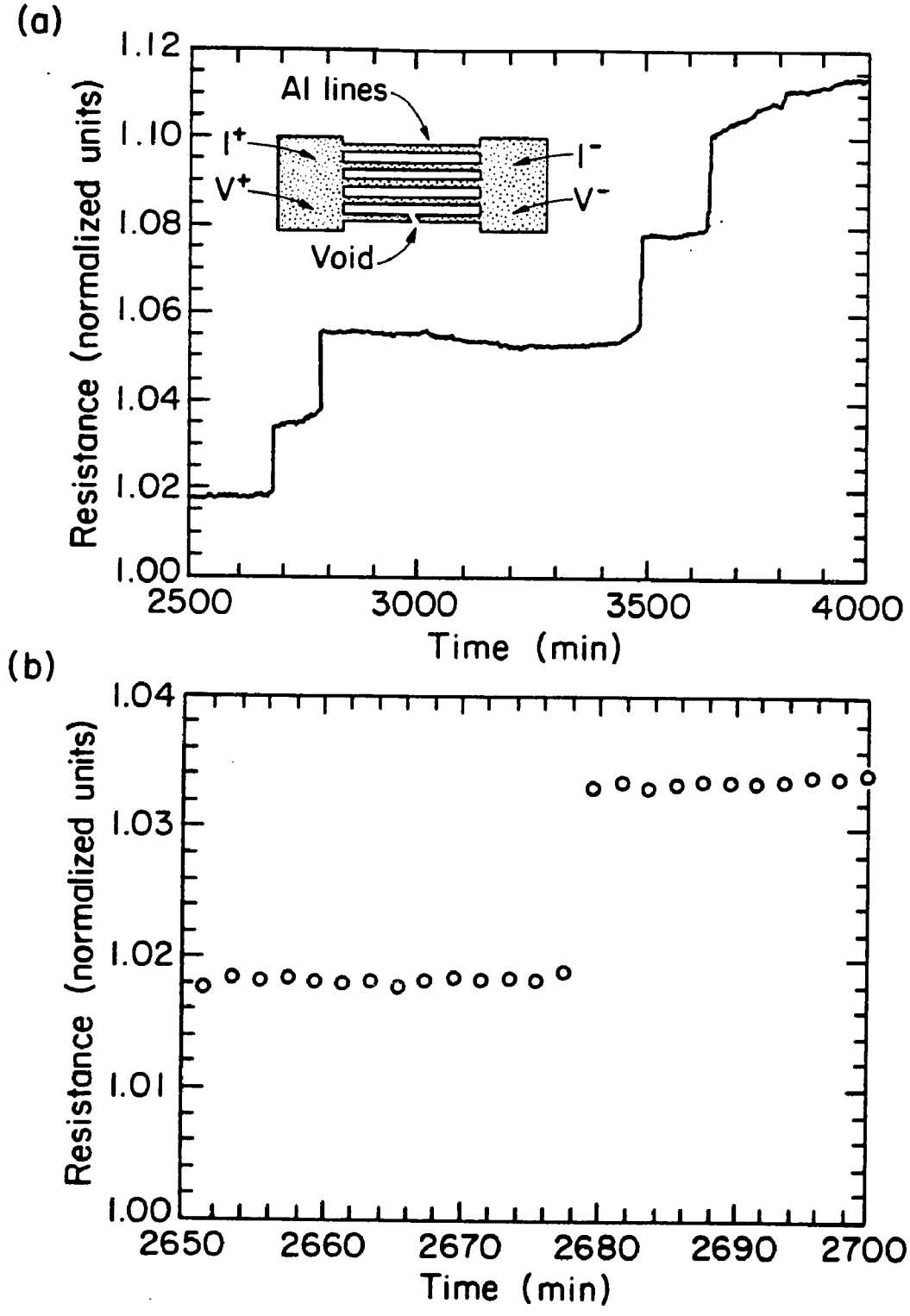

Fig. 2.8 A plot (a) of resistance vs. anneal time of a grid of (1 μm wide) Al lines. The abrupt increases are speculated to be due to voids forming in individual lines causing a complete break (discontinuity) within that line. A plot (b) of the change at t≈2678 min on an expanded scale shows the individual data points and indicates that the break (void formation) in the line occurs in short period of time (≈1 min).

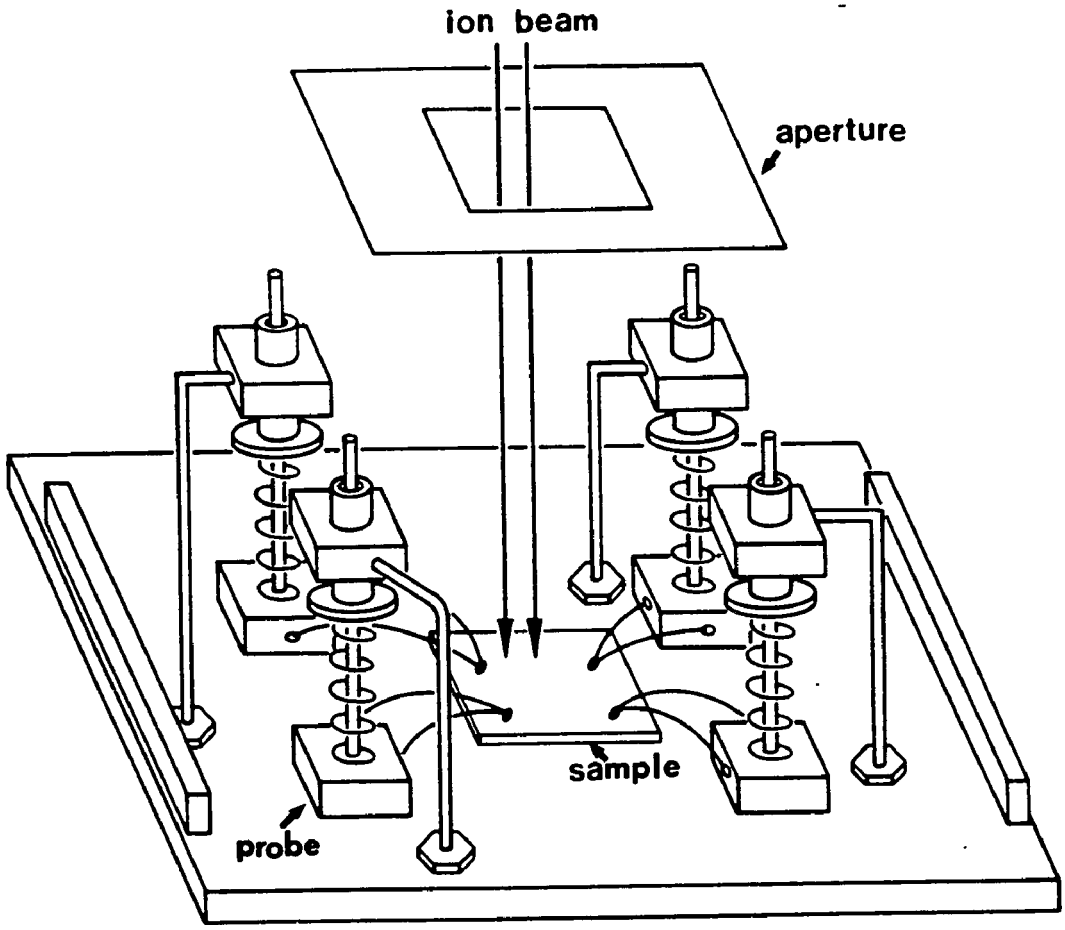

Fig. 2.9 In-situ resistance apparatus used for monitoring ion beam mixing.

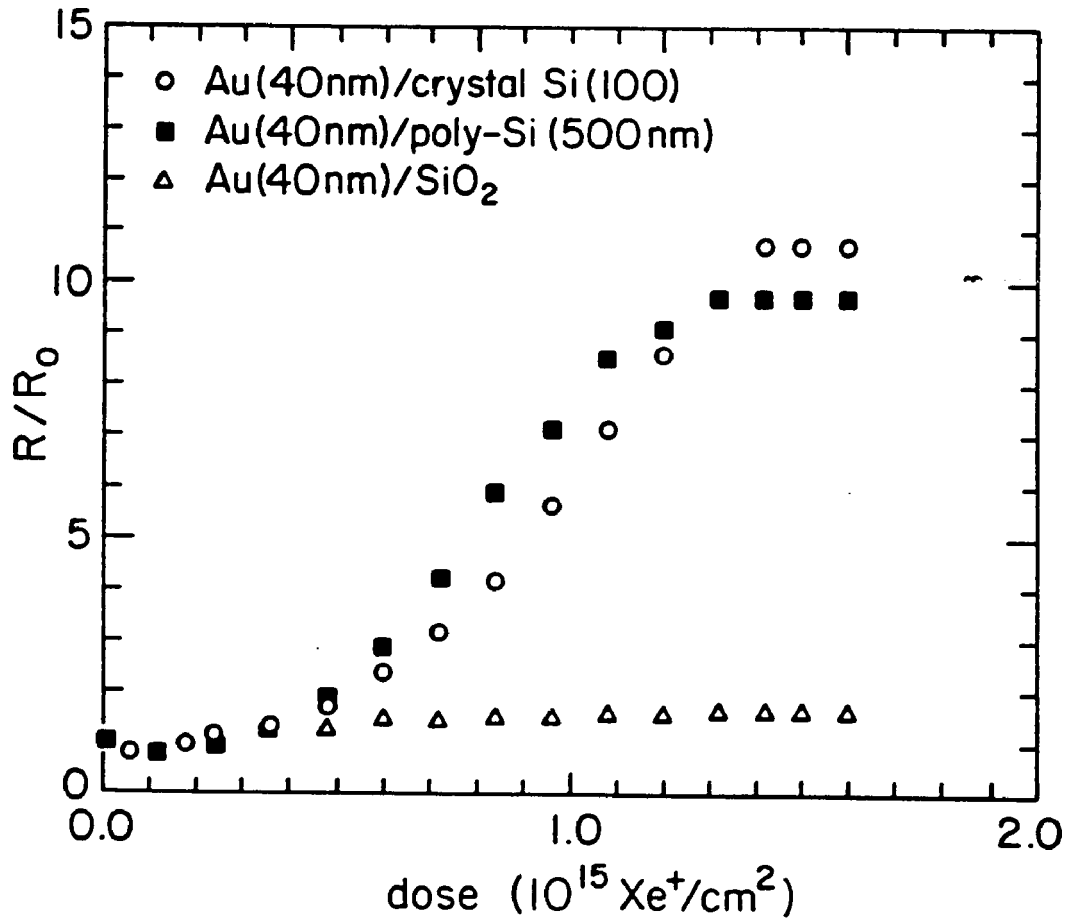

Fig. 2.10 Sheet resistance vs. ion dose during ion beam mixing of Au on crystal Si, polysilicon and SiO_2.

2.5 References

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Chapter 3

Two dimensional Si crystal growth during thermal annealing of Au/polysilicon bilayers.

3.1 Introduction

The reaction between Au and polysilicon is related to two topics of interest in the study of electronic materials. The first area relates to the stability of metal/Si contacts, which is associated with reliability issues in electronic devices. This is particularly relevant in VLSI applications of PtSi/polysilicon contacts to the emitter of bipolar transisters[1]. The second area of interest is the growth of Si crystals in the solid phase[1a,2], which is related to work on Si lateral solid-phase-epitaxy growth, currently being investigated for possible applications in three-dimensional integrated circuits[3]. There are two general classes of metals in metal/polysilicon systems[4,5]: those metals which form stable silicide phases (e.g., WSi_2, $MoSi_2$, PtSi, etc.,) and those which form eutectics with Si including Au(360°C), Ag(830°C) and Al(577°C). Reactions in the eutectic systems result in the formation of large grained Si[6-8].

Most work involving thermal reactions in the Si eutectic systems has been done on the Al/polysilicon system[9]. Experiments[10-12] have demonstrated the growth of Si crystallites during thermal anneals of Al and polysilicon over a wide range of Al/Si thicknesses. The Al/Si system was

configuration of amorphous Si /Al/Si substrate.

This study investigates the structure of the Si crystallites formed during thermal annealing of Au/polysilicon bilayers, where the thickness of the Au layer is less than the polysilicon layer. This reaction [16,17] produces large-grained Si crystals, as was found in the Al/Si system. The unique characteristic of the Au/Si system is that the grain growth of Si occurs at relatively low temperatures (≈300°C), as compared with the typical crystallization temperature of amorphous Si (≈500-600°C)[1a]. We focus the analysis on the Si by characterizing the location, size, shape, and orientation of the crystals. Analyses include x-ray diffraction (XRD), scanning electron microscopy (SEM), and planar and cross-sectional transmission electron microscopy (TEM).

This chapter[23] deals with the end state of the reaction, describing the process in terms of the redistribution and other time-independent characteristics of the components: Au, polysilicon and crystal-Si (c-Si). The following chapter investigates the time and temperature effect on crystal growth and discusses the rate-limiting processes that control the kinetics of the reaction.[18]

3.2 Sample Preparation

Au/polysilicon bilayers were fabricated on inert substrates including quartz wafers and thermally oxidized single-crystal Si substrates. Polysilicon was deposited by the low pressure chemical-vapor-deposition process (LPCVD) at 620°C to a thickness of 100 to 400 nm. The polysilicon thin films had columnar grain structure, which is typical for films grown with

LPCVD at this temperature[19]. After cleaning the surface of the polysilicon with a buffered hydrofluoric-acid solution, Au was thermally evaporated onto the polysilicon thin films at a pressure of $5x10^{-6}$ Torr to a thickness of 80 to 250 nm.

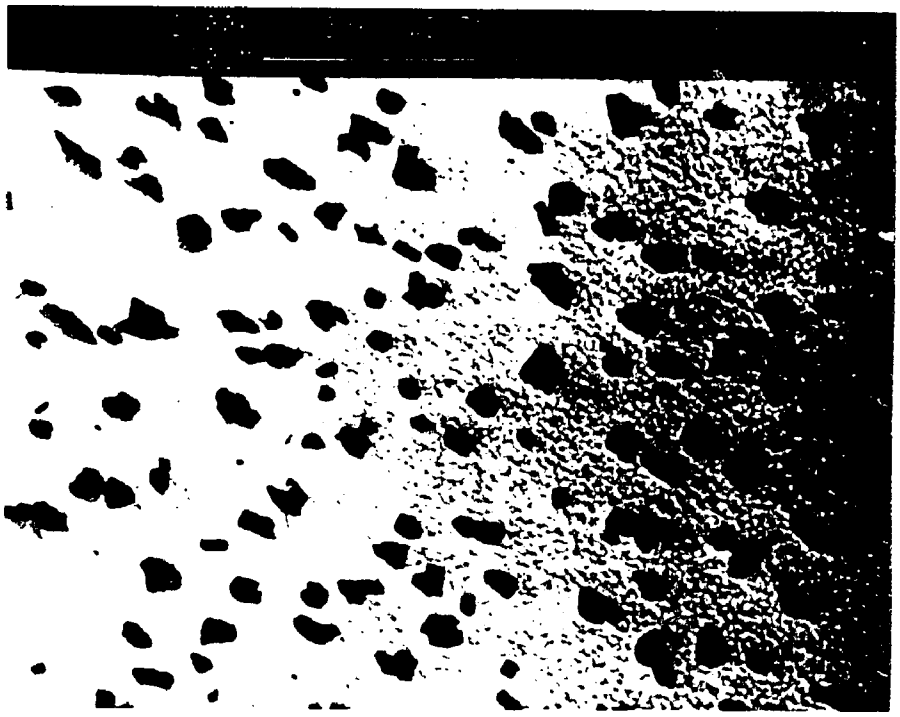
Samples fabricated on quartz substrates were used in obtaining XRD data since diffraction from this substrate would not interfere with the XRD intensities generated by the polysilicon and crystal-Si thin films. Samples needed for planar TEM investigations were made by first removing the polysilicon from the SiO_2/Si substrate prior to Au deposition. This was done by lifting off the polysilicon by using a concentrated hydrofluoric-acid solution. Cross-sectional TEM analyses were made on the Au/polysilicon layers that were deposited on thermally oxidized Si substrates.

3.3 Si crystal growth during thermal annealing

The Au/polysilicon bilayers were annealed in an vacuum system maintained at a nominal pressure of $1x10^{-7}$ Torr at 270°C. The appearance of Si crystal was easily observable via SEM imaging using a JEOL™ 35 system. SEM micrographs of a partially annealed sample are shown in Fig. 3.1. The Si crystals appear as faceted dark patches; the contrast is due to the two different elements at the surface (Au and Si). The area of each crystal depends on the duration of the anneal, but eventually, they impinge on one another, displacing the entire original Au layer, leaving the top layer as a "patchwork-quilt" network of crystal-Si plates.

A cross-sectional TEM micrograph of a partially annealed sample is shown in Fig. 3.2. The initial thickness of the Au was 170 nm and the

(a)



(b)

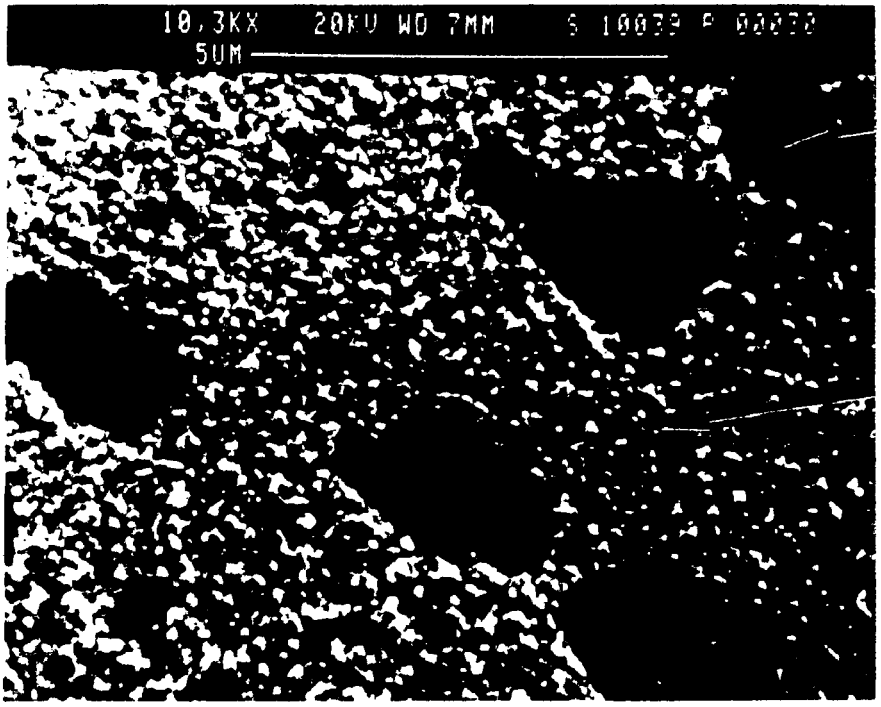


Figure 3.1 SEM photograph of Au(≈170 nm)/polysilicon(≈400 nm)/SiO_2 after 270°C vacuum furnace anneal for 240 min.

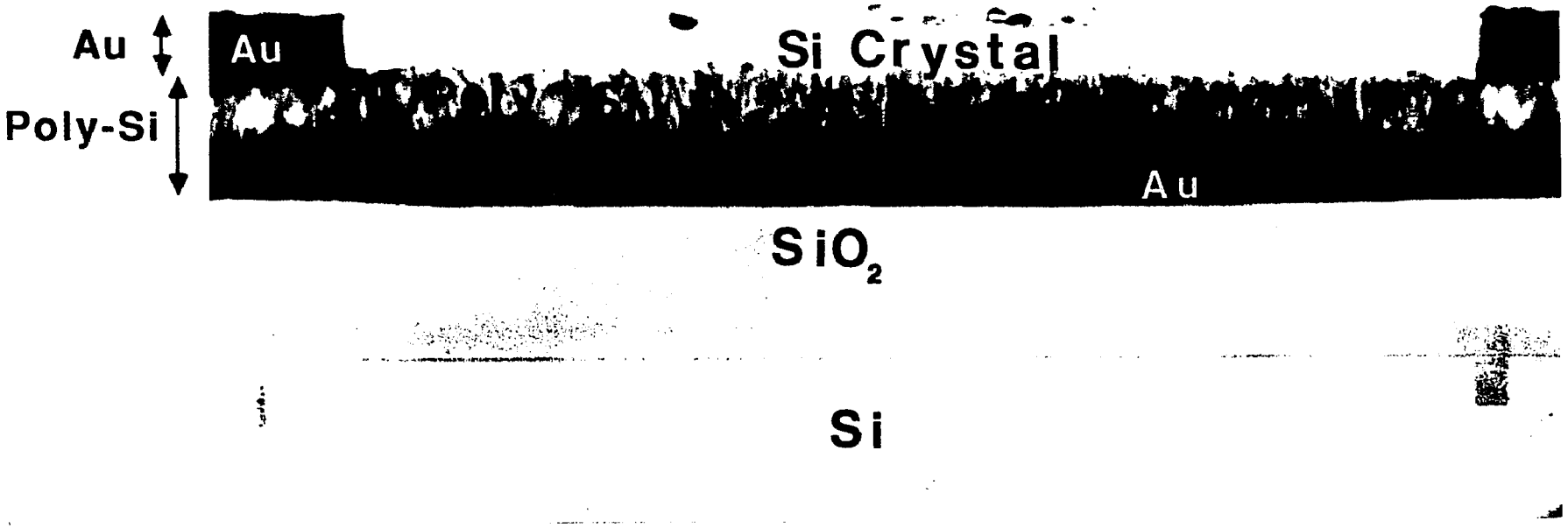


Figure 3.2 Cross-sectional TEM data of Au(≈200 nm)/polysilicon(≈400 nm)/SiO_2 sample after 250°C vacuum furnace anneal.

polysilicon was 400 nm thick. The Au appears as the dark areas in the TEM micrograph. The Si crystal, shown in the micrograph, has the shape of a flat plate having a thickness equal to the original Au layer and is supported from below by the underlying polysilicon layer. During the anneal the Au/Si interface at the edge of the crystal moves laterally in the direction of the Au layer; the velocity of this interface determines the growth rate of the crystal. There are no observable inclusions of Au within the crystal.

During the growth of the Si crystals the Au redistributes by vertically penetrating the polysilicon layer and accumulating at the bottom of the polysilicon layer. Accumulation of Au at the bottom polysilicon/SiO_2 interface is expected since the Si at this interface is more disordered (smaller grains) and should dissolve more easily into the Au as compared to the subsequent layers of Si that eventually form larger columnar grains. The three-dimensional distribution of the Au after annealing was directly observed by etching the entire sample in a hydrofluoric- and nitric-acid solution. This solution dissolved the Si and SiO_2 releasing the Au from the substrate as an isolated, free-standing, completely intact Au film , which was then analyzed via SEM. The Au and Si displace each other in such a way as to keep the entire thickness of the composite layer constrained to the original geometry of the sample. No voids or "hillock" formation were observed.

The Si crystal plates can also be observed in planar view via SEM by removing the Au layer using a potassium iodide (KI) solution. The crystal shown in Fig. 3.3a was grown with Au/polysilicon bilayers deposited onto a flat substrate. The crystal shown in Fig. 3.3b was prepared on a substrate that had a stepped surface, and it demonstrates that the shape of the crystals follows the contour of the original Au/polysilicon bilayer deposited across the

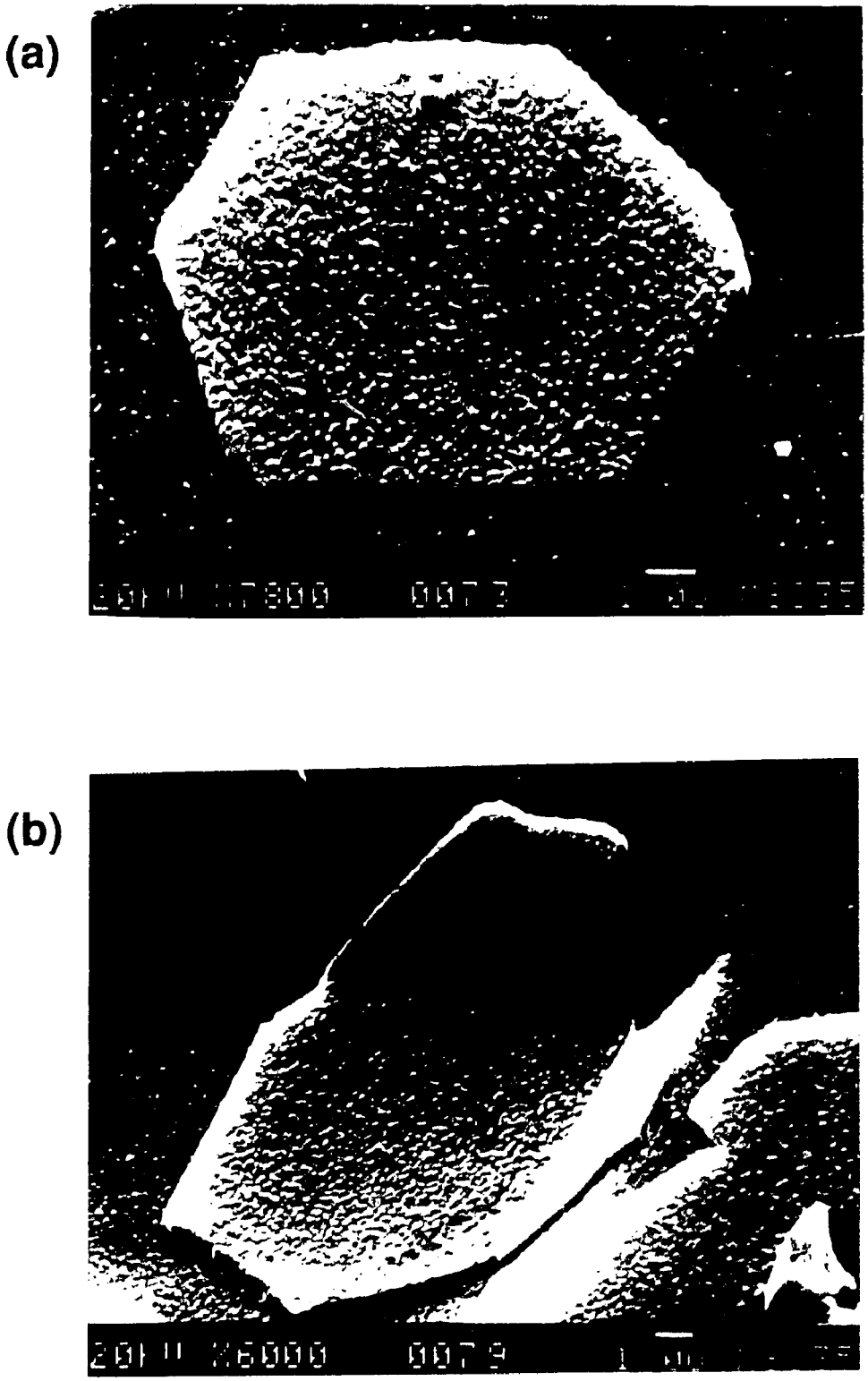


Figure 3.3 SEM micrograph of Si crystals on polysilicon after Au was selectively etched. Au(≈250 nm)/polysilicon(≈400 nm)/SiO_2 samples were fabricated on flat (a) and stepped-surface (b) substrates.

step. Preliminary cross-sectional TEM investigation of this type of obtuse crystal indicate that it is one complete crystal. Apparently, the lateral growth of the crystals is not restricted to flat surfaces. This conformal crystal-growth process may provide possibilities for growing single crystals of unusual shapes.

Si crystal growth was also observed during *in-situ* annealing in the TEM. The redistribution of the Au during the annealing allowed the Si crystals to be seen via bright-field (BF) imaging. Two samples, with different Au thicknesses where made. As expected, the sample with the thicker (200 nm) Au layer produced thicker Si crystals (Fig. 3.4a), as is evident from the presence of Kikuchi patterns (Fig. 3.4b) This is compared to the diffraction pattern of the thin Si crystals (Fig. 3.4c) formed with a thinner (80 nm) Au layer which shows a diffraction spot pattern (Fig. 3.4d).

The redistribution of the Si was also analyzed on annealed samples which had the Au chemically removed using a KI solution. A TEM planar view micrograph (Fig. 3.5c) shows three distinct regions in the vicinity of a crystal. The first region is the polysilicon area far away from the crystal. The selected-area-diffraction (SAD) pattern of this area, shown in Fig. 3.5a, is similar to the SAD pattern obtained from the original unreacted polysilicon layer, indicating minor, if any, change in the polysilicon layer in this area. The second region is the crystal area. The SAD data taken from this area with an aperture much smaller than the crystal are shown in Fig. 3.5b, consisting of Debye rings generated by the polysilicon superimposed on a Kikuchi pattern generated by the Si crystal. Both Kikuchi and Debye-ring diffraction patterns appear together because both the crystal and the underlying bed of polysilicon diffract the electron beam. Because of the size of the aperture, only the polysilicon under the crystal will diffract the beam.

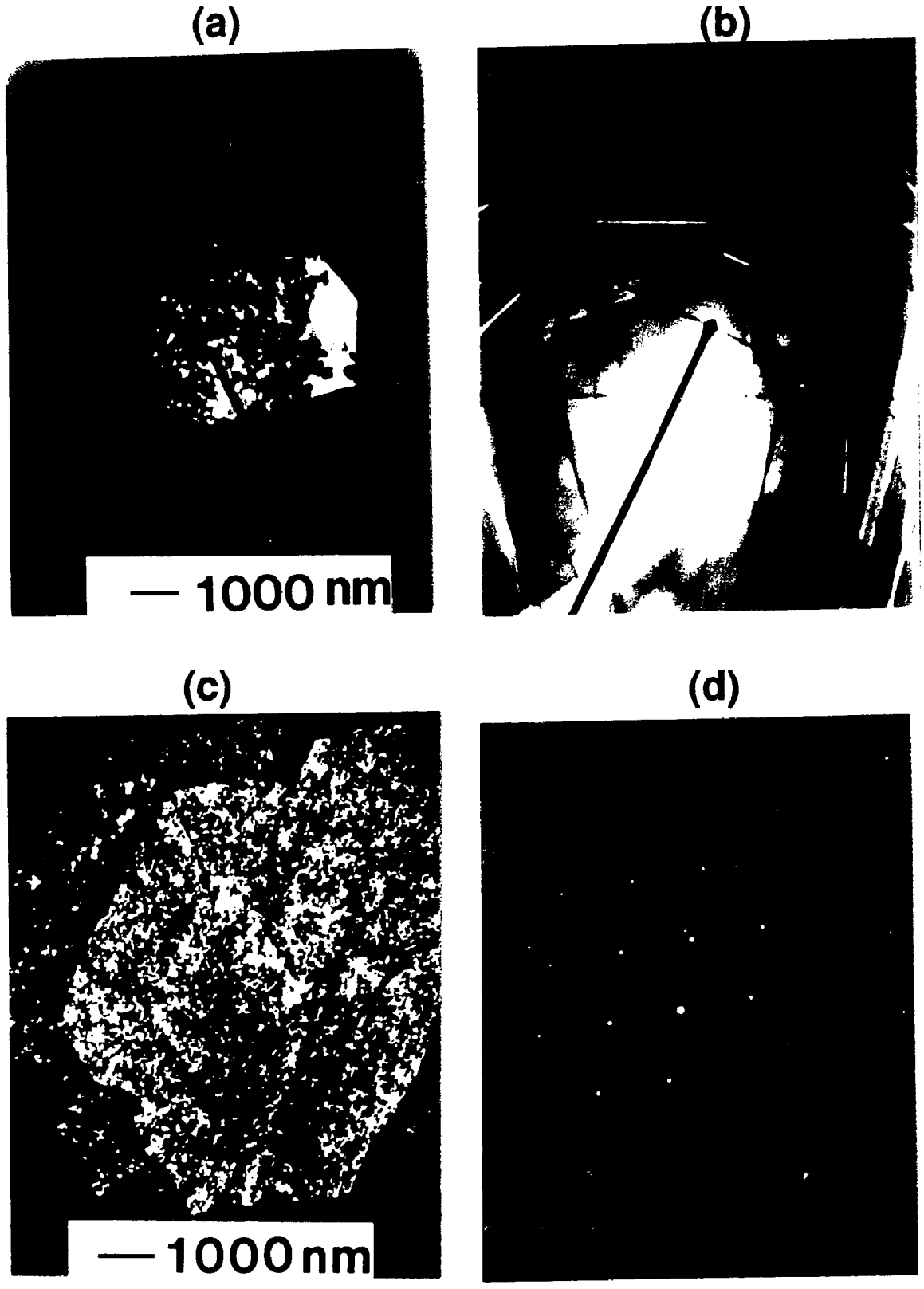


Figure 3.4 BF image and diffraction micrographs of thick (a,b) and thin (c,d) Si crystals. The sample were made with thick (a,b) (200 nm) and thin (c,d) layers of Au on Si(100 nm). The Au/polysilicon samples were annealed (250°C-300°) in-situ in the TEM.

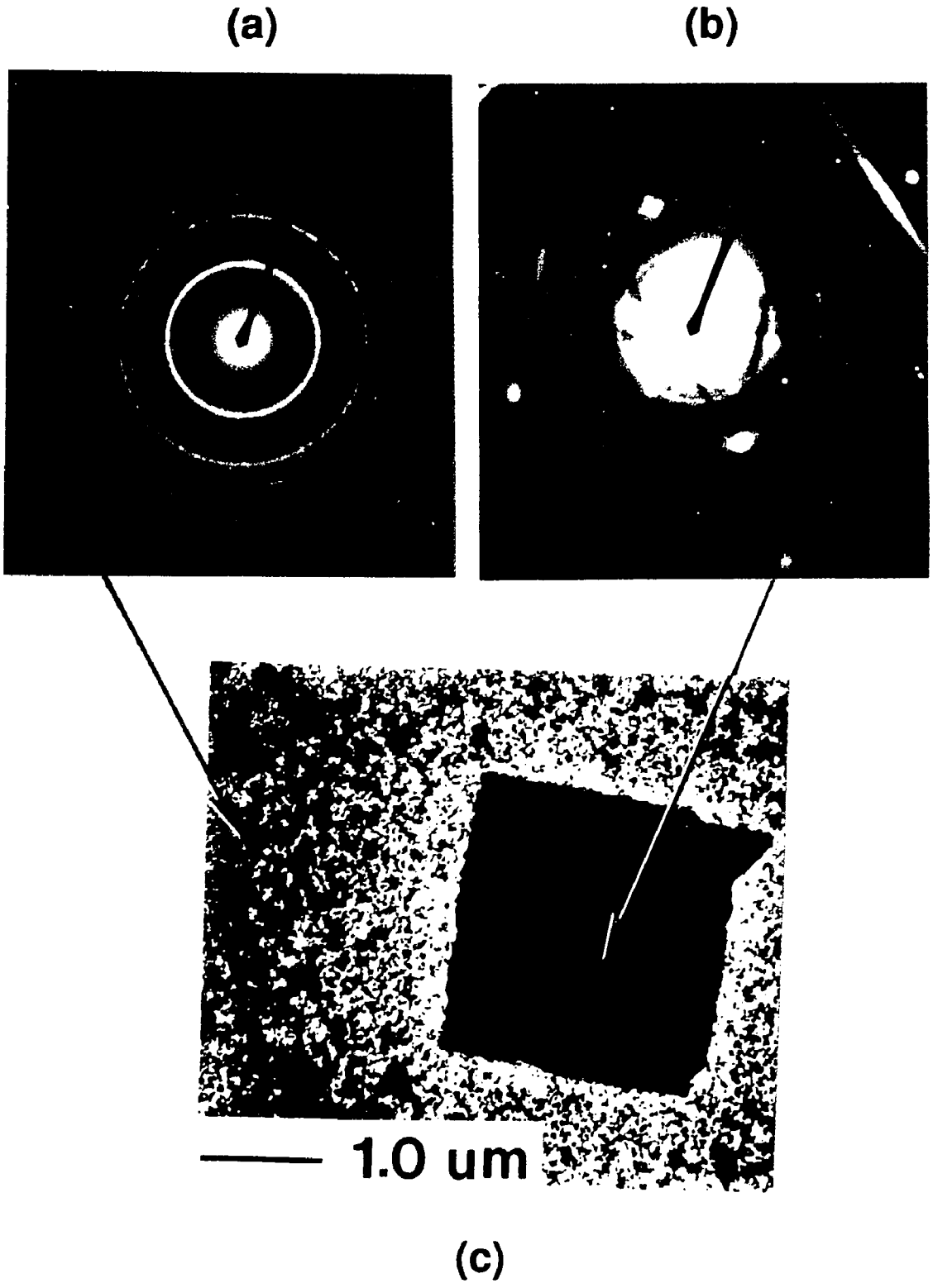


Figure 3.5 Planar TEM data of Au(200 nm)/polysilicon(100 nm) in-situ annealed sample after Au was etched showing Si depletion in area adjacent to crystal: Debye rings (a) from the polysilicon, Kikuchi pattern and Debye rings (b) from the crystal and polysilicon, and (c) BF micrograph.

The third region is the area laterally adjacent to the crystal. The variation of the BF intensity near the edge of the crystal, shown in Fig.3.5c, qualitatively indicates the extent and lateral range of Si depletion from the polysilicon film due to the lateral transport of Si from the polysilicon layer to the crystal. The Si that makes up the crystal was transported over distances of several microns.

The Si crystals grown from the Au/polysilicon bilayers did have crystalline imperfections. Bright-field (Fig 3.6a) and dark-field (DF) (Fig. 3.6b) images of an annealed sample, after the Au was removed, indicate the presence of defects (e.g., twins) in a thin (100 nm) Si crystal.

Throughout this investigation no metastable phases of Au-Si were identified. The major phases present via TEM and XRD evaluations were Au and Si.

3.4 Orientation of the Si crystals.

The Au/polysilicon reaction was also analyzed with XRD using a SCINTAG™ diffractometer. Analysis was complicated by the condition that both the Si crystals and the polysilicon had preferred orientation. Consequently, the relative tilt of the sample during XRD experiments is important when comparing different samples and different peak intensities. One particular method which analyzes peak intensity as a function of sample orientation is the pole figure method[20]. This method maps the intensity of a given set of {hkl} poles as function of the orientation (tilt Ψ and rotation ω) of the sample.

Pole figure data were taken with the Si 220 reflection on unannealed

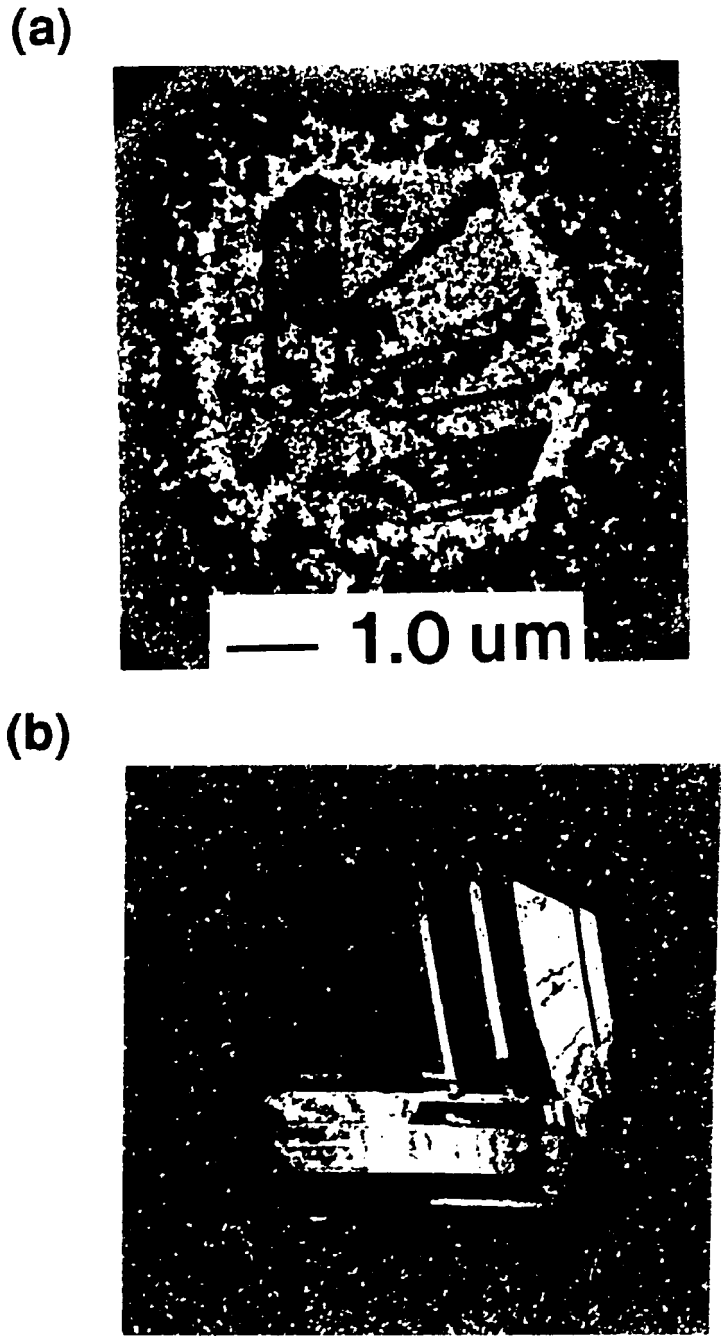


Figure 3.6 BF (a) and DF (b) TEM micrographs of Si and polysilicon after Au selective etch. The Au(≈100 nm)/Si(≈100 nm) samples were annealed in-situ with the TEM.

samples and showed that the distribution of the {110} poles was not random but concentrated at zero tilt ($\psi = 0°$), indicating that the grains had a (110) preferred orientation. This result was expected since polysilicon films grown at 620° typically have (110) preferred orientation.[19] The same pole figure routine was applied to annealed samples and showed that the new crystals have the same (110) orientation as the as-deposited sample. The intensity of the 220 reflection is highest at zero tilt ($\psi = 0°$), as shown in Fig. 3.7a, with the majority of the grains aligned to within 13 degrees ($\Delta\psi \approx 13°$) of the normal to the surface. The pole figure method was also applied to the annealed samples using the Si(111) reflection and the distribution of intensity is shown in Fig. (3.7b). The maximum intensity for the (111) reflection occurs when the sample is tilted ($\psi \approx 30\text{-}40°$) off normal, which again confirms the (110) preferred orientation since the (110) and (111) poles in the crystal are separated by an angle of 35.3°. The uniformity of the intensity vs. rotated angle ω indicates that the Si plate crystals are randomly oriented about the (110) pole, indicating [110] fiber texture.

The (110) preferred orientation of annealed samples was confirmed qualitatively with TEM by a random inspection of crystals. The (110) diffraction pattern was the most frequently obtained pattern when the sample tilt was restricted to a limited range about the sample normal. The BF image (Fig. 3.8a) and diffraction pattern [Fig. (3.8b)] were obtained from one particular (110)-oriented crystal, where the sample was tilted ≈11° off the sample normal. The same (110) diffraction pattern was obtained at all tested locations of this crystal without any additional changes in tilt, which confirms that the crystal is indeed a single crystal. The features in the micrograph in the area framed by the crystal are not due to the crystal, which is essentially transparent, but are due to the material beneath the crystal:

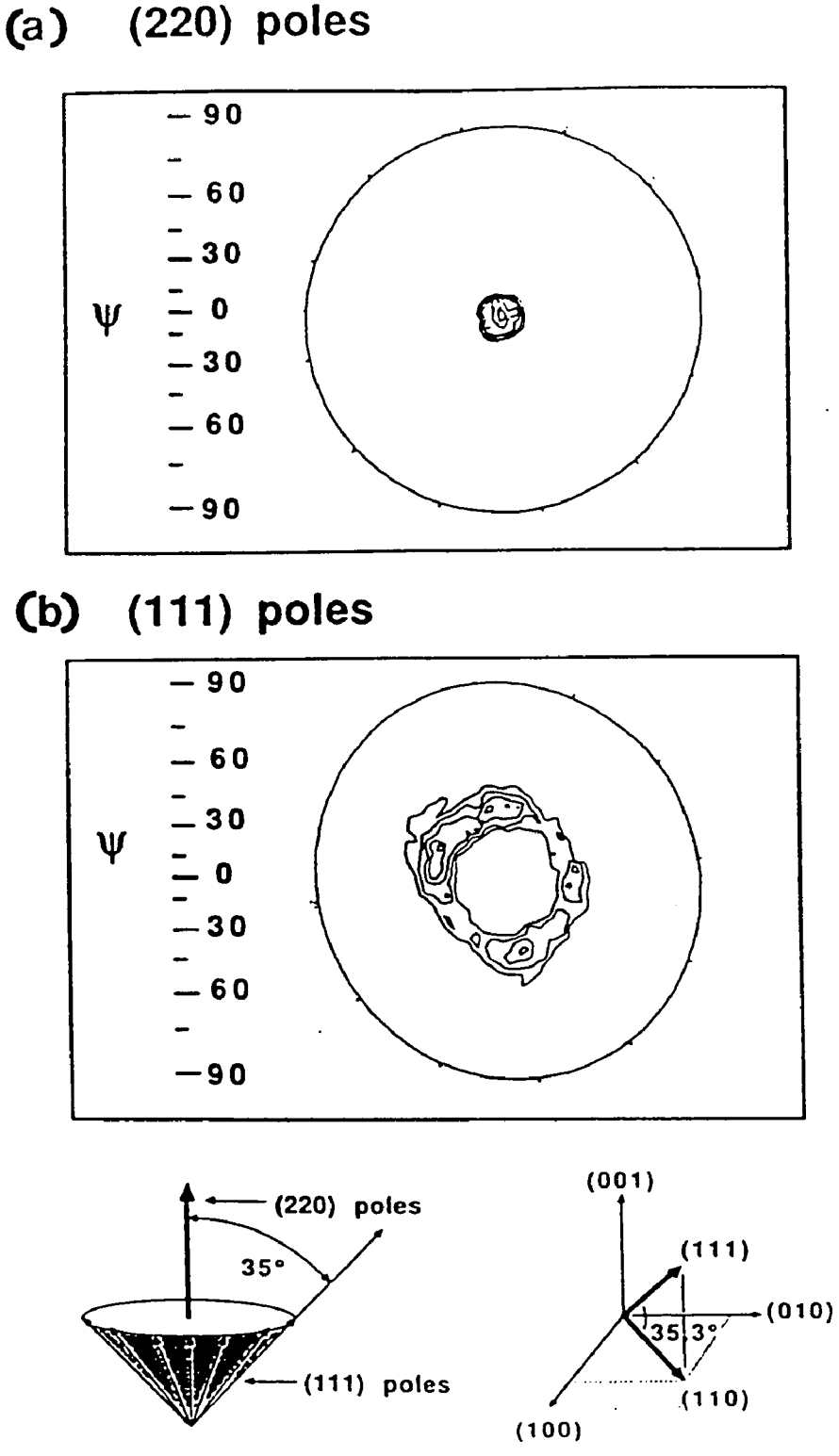


Figure 3.7 (220) and (111) Pole figure data showing [110] fiber texture of the annealed Au(≈200 nm)/polysilicon(400 nm) sample. The {220} poles are concentrated near the vertical $\psi=0°$ and the {111} poles concentrated at an off axis tilt angle (ψ≈30-40°).

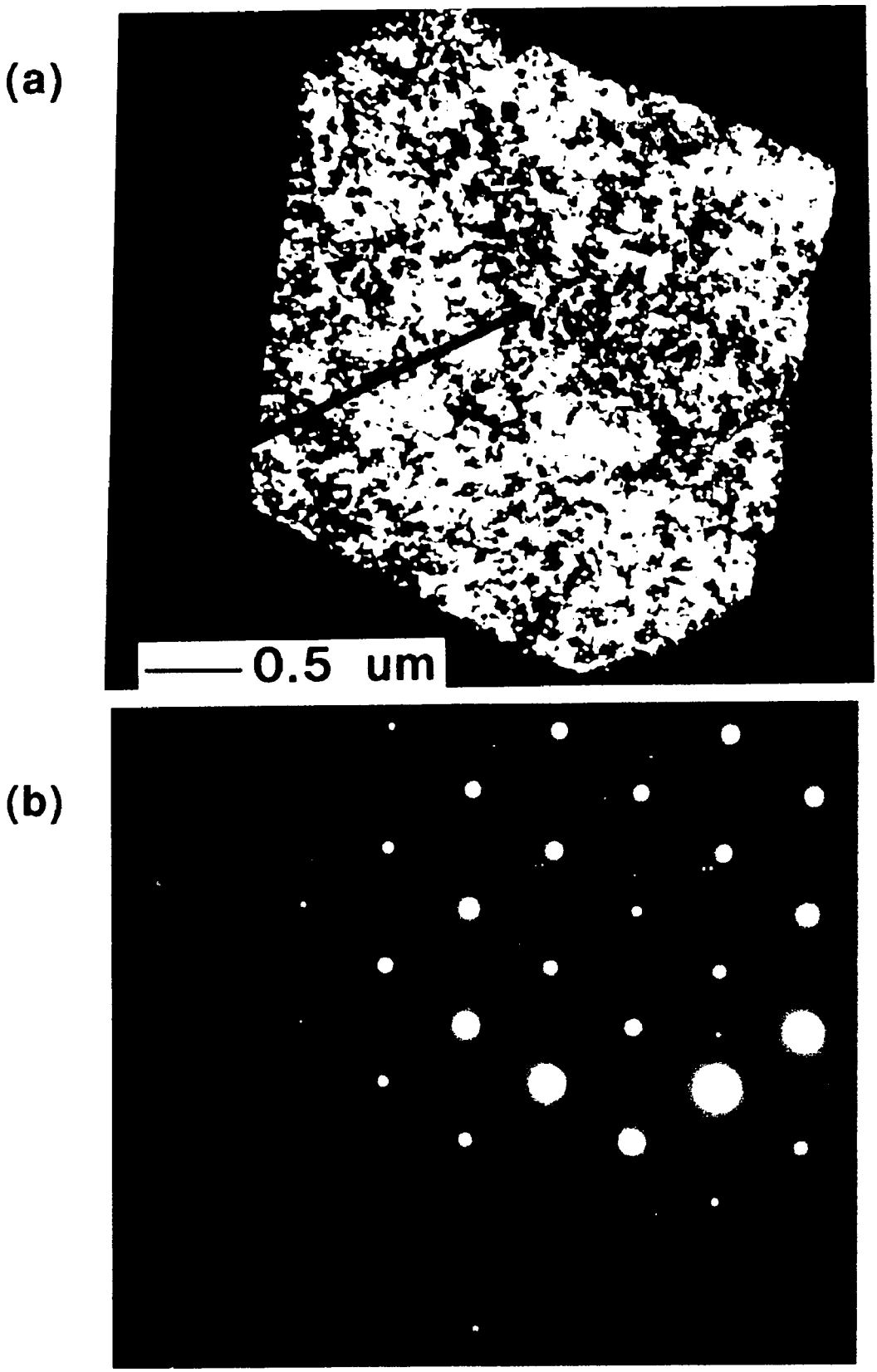


Figure 3.8 TEM planar micrograph (a) and diffraction pattern (b) of the (110) pole of crystal oriented within 12° from the normal of the sample surface. Au(150 nm)/polysilicon(400 nm) sample after in-situ anneal in TEM.

the remaining polysilicon and Au which has penetrated the polysilicon film. There were crystals which did not have the (110) orientation, but they were the exceptions.

Although the orientation of the unannealed and annealed samples were similar, there were two significant differences in the XRD data between the annealed and unannealed samples: an increase of XRD intensity (increase) and a small shift (decrease) in the 2θ position of the 220 reflection. The increase of peak intensity (Figs. 3.9b and 3.9c) is attributed to the increase size of the Si crystal during annealing. The decrease in the 2θ ($\Delta 2\theta \approx 0.12°$) position of the (220) reflection was observed [Fig. (3.9b)] when unannealed and annealed samples were compared. All XRD data were taken with a collimated beam to ensure reproducible sample areas. To reduce other measurement errors, the raw data were corrected for the $K\alpha_1$ and $K\alpha_2$ doublet convolution and adjusted to obtain absolute peak position by using the Au(111) reflection generated by the Au in the sample (an internal reference source). Additional confirmation of changes in peak position were obtained from XRD data collected from a partially annealed sample which shows (Fig. 3.9d) two resolvable (220) Si peaks ($\Delta 2\theta \approx 0.08°$). Assuming that the instrumentation effects have been eliminated, the peak shifts are then attributed to a change in the Si crystal lattice parameter(s).

3.5 Discussion

Large, 2-dimensional, platelike Si crystals are formed from fine-grained polysilicon when bilayers of Au/polysilicon films are thermally annealed. The discussion focuses on the thermodynamic factors in the system which

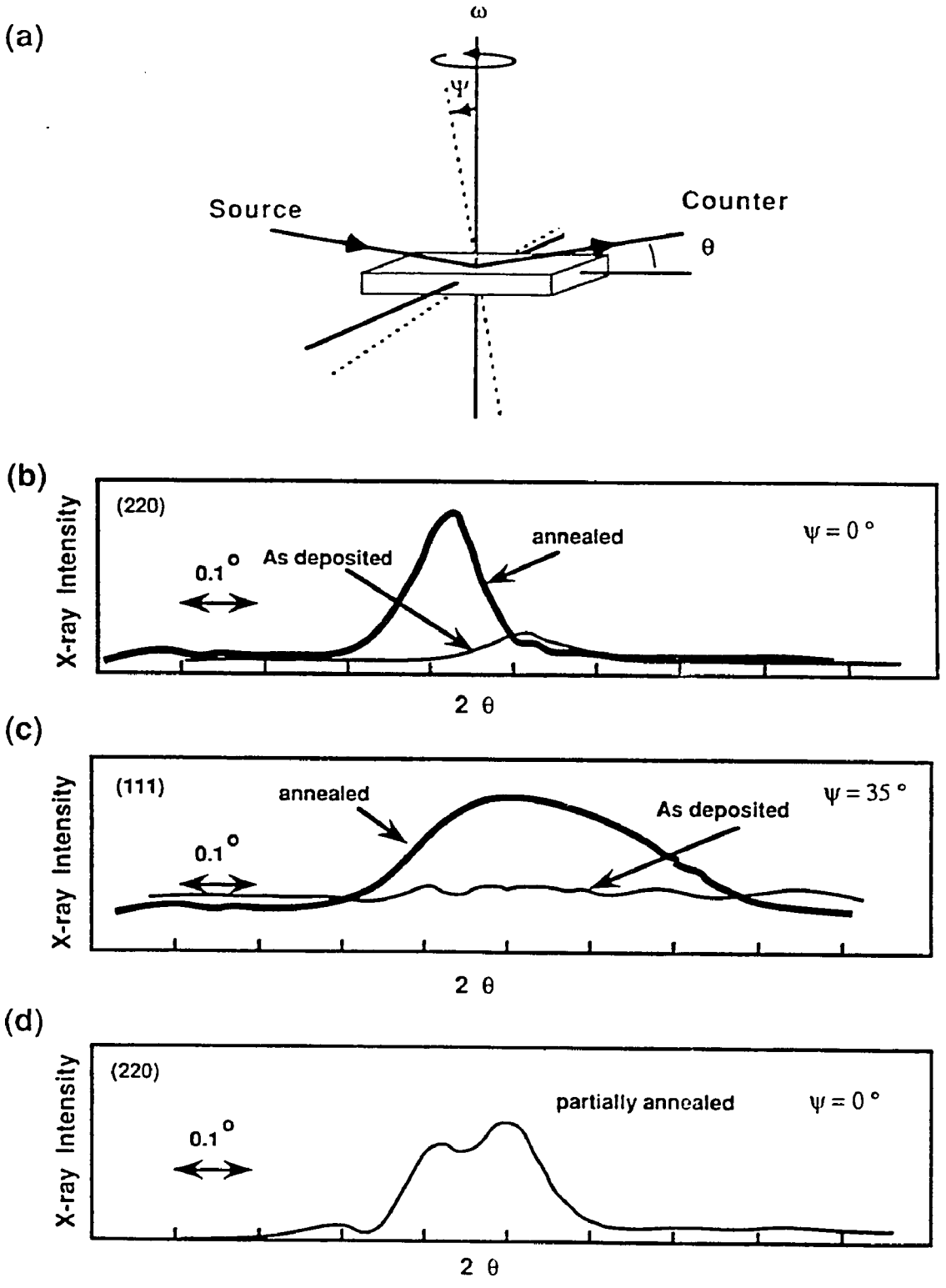


Figure 3.9 XRD data of annealed and as deposited samples (a) near (220) peak with sample at ψ=0°, (b) near (111) peak with ψ=35° and a partially annealed sample at ψ=0°. Data indicate shift in peak position.

drive the reaction and the origin of the large crystals.

In discussing the thermodynamic factors, we begin by noting that the main result of the reaction is the increase (by a factor of ≈ 10,000.) of the size of the Si grains. The composition of the starting reactants and the final products are the same: Si crystals. Therefore, the thermodynamic factors of the reaction must center on a discussion of the microstructure of the initial polysilicon film.

The CVD (620°C) method forms crystals under extremely non-equilibrium conditions. The free energy of these films is higher than that of a single crystal because of the internal interfaces (grain boundaries, twins, etc.,) present in the initial polysilicon layer. This difference in free energy is quantified by modelling the polysilicon film as a mosaic of small crystals (300 Å diameter) interfaced with one another at large-angle twist/tilt grain boundaries. The internal interface energy σ_i at a large-angle grain boundary can be estimated, given a value for the surface energy $\sigma_s \approx 1$ J/m^2 for Si, by using the relationship[21] $\sigma_i \approx 1/3\ \sigma_s$. From this calculation, we estimate the normalized (over all atoms in the film) free-energy difference due to the internal interface energy to be of the order of ≈0.01 eV/atom. We believe that this difference in free energy is responsible for the overall recrystallization process.

Recrystallization does not readily occur in the as-deposited polysilicon films when annealed at temperatures below 1000°C. In contrast, when Au is deposited on the polysilicon surface, recrystallization occurs at temperatures as low as 200°C. The difference is due to the kinetic factors in the bilayer system, where the Au layer provides a fast diffusion path for the transport of Si.

We have shown that the crystal growth proceeds via the lateral

transport of Si through the Au. Consequently, there must be differences in the chemical potential μ_{si}. of the Si from place to place (laterally) across the film. This gradient $\nabla\mu_{si}$ is believed to be present in the as-deposited film and occurs because of physical differences (shapes) between the crystals, which are exposed to Au at the Au/polysilicon interface. There is a wide variation[19] in the size of crystals that form the polysilicon layer. Assuming that smaller crystals have a larger surface curvature than the larger crystals, it can be deduced from the Thomson-Freundlick[21] relationship that the chemical potential of the Si at the small-grained crystal surface should be higher than for the large- grained Si. This reaction then can be viewed as a form of Ostwald ripening. The Si concentration in the Au will be higher near the small-grained (high curvature) crystals as compared to the large-grained (lower curvature) crystals. The small-grained crystals will dissolve and the large-grained crystals will grow.

The final topic of this discussion deals with the initial stages of the reaction and analyses the origin of the growing crystals. Although it would seem possible for nucleation of Si to occur since there are areas of local supersaturation of Si in the Au, we do not think nucleation of Si grains plays a significant role in this reaction for two reasons. First of all, it does not seem reasonable from energy considerations that a nucleated Si crystal could grow faster than the much larger Si grains that already exist. The second reason deals with the orientation of the growing crystals. If the reaction proceeds with only grain growth and negligible nucleation, then the orientation of the initial set of grains would be the same as the final set of large grains. This is what was observed experimentally with the XRD pole figure data. The distribution and orientation of the (110) poles of the as-deposited sample were the same as the annealed large-grained sample.

To further investigate the orientation relationship between the growing crystal and the substrate on which it grows, another experiment was performed[22]. A special sample was made for this experiment. Starting with the same polysilicon/SiO_2/Si substrate, the polysilicon and SiO2 layer were removed (etched) from half of the sample, which exposes the (100)Si wafer on the other half of the sample. Au was then deposited over the entire wafer, allowing for a continuous Au film to laterally connect the polysilicon side of the sample with the single-crystal (100) wafer side of the sample. During thermal annealing of this sample, Si was transported laterally (via the Au layer) from the poly Si side to form individual Si crystals on the Si(100) side of the sample. These crystals are in the shape of right-angle prisms, which is the form expected of a growing (100)Si crystal, where the (111) prism faces are the slowest growing sides of the crystal. All these crystals have the same physical orientation with respect to the substrate..

In both cases (Au/polysilicon or Au/single crystal) the orientation of the growing crystals emulates the orientation of the crystal at the surface it grows on. We deduce from these data that the origin of these crystals is due to the growth of already existing grains at the initial Au/Si interface and that nucleation is not significant.

A description of the overall process of the formation of the large-grained Si crystals in the Au/polysilicon is now suggested. After Au deposition the top-surface Si crystals begin to interact with each other. The Au layer acts as a short-circuit diffusion path for the Si. The average Si concentration in the Au will be below the solubility limit for the small grains (large curvature), so they will begin to dissolve, but Si concentration will be beyond the solubility limit for the large grains (small curvature) and they will begin to grow. The sequence for the growth process is illustrated in Fig. 3.10.

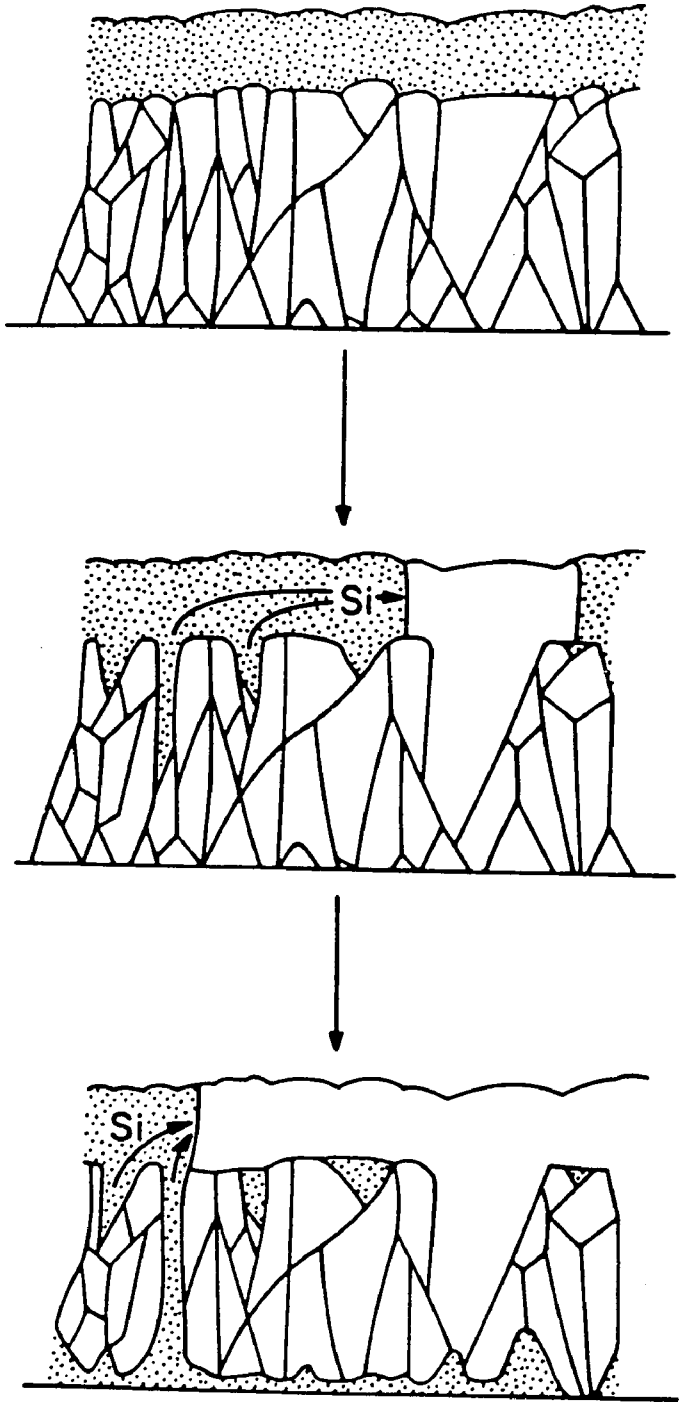


Figure 3.10 A diagram showing the stages of grain growth of Si crystals. The initial structure is a bilayer of Au (top) and of polysilicon with various grain sizes (bottom). Note that the resultant large crystal has the same orientation as the initial grain.

Initially, the already existing large grains grow upward from the interface in a 3-D manner until they impinge on the top Au surface, and then they grow in a 2-D manner radially to form two-dimensional platelike crystals. The growing Si crystal displaces the Au. Competition between the large grains will determine the final number/size of the grains. This topic will be investigated in the following chapter which focuses on the kinetic characteristics of this reaction.[18]

3.6 Conclusions

We have observed and analysed the interaction between bilayers of Au and polysilicon. The grain size of the Si can increase by a factor of 10,000 from the fine-grained polysilicon to large two-dimensional single crystals upon thermal annealing at temperatures between 200 and 300°C. The large crystals have the same (110) preferred orientation as the fine-grained polysilicon.

Ostwald ripening (grain coarsening) is the basic process responsible for the formation of the crystals. Large grains of the initial polysilicon film grow at the expense of the small grains. The Au film provides a fast diffusion path for Si transport. Si from small grains dissolves into the Au layer, and then diffuses to the large crystal, which may be several microns away. The Au/polysilicon bilayer configuration allows for a unique two-dimensional growth process to occur, which gives rise to the possibility of growing arbitrarily shaped, two-dimensional, nonflat Si crystals.

The driving force for this small-grained to large-grained transformation is attributed to be the reduction of the free energy associated with the

interface energy at the polysilicon grain boundaries. The origin of the crystals is concluded not to be nucleation, but rather the growth of already existing large grains (small curvature) initially at the Au/polysilicon interface.

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Chapter 4

Kinetic study of Si recrystallization in the reaction between Au and polysilicon films

4.1 Introduction

The formation of large Si crystals has been observed [1] during thermal anneals of Au/polysilicon bilayers. These Si crystals are formed at much lower temperatures (T ≈300°C) than the typical recrystallization temperature[2] of the polysilicon (1000°C) without gold. Experiments have shown that Si dissolves into Au and diffuses rapidly through Au at temperatures well below the Au/Si eutectic[3] (365°C) to achieve recrystallization.

It was shown in the accompanying paper[1] that thermal annealing of Au/polysilicon bilayers produced flat, two dimensional Si crystals (c-Si), of thickness equal to the thickness of the original Au layer. These crystals are the result of the growth of an already existing grain located at the initial Au/polysilicon interface which grows upward into the Au until impinging the top surface, and then grows radially in the shape of a two dimensional plate-like crystal. Supply of Si from the surrounding polysilicon layer to the crystals occurs through the long range transport of Si through the Au layer. One to one displacement of the Au by the Si keeps the total thickness of the sample constant and uniform. The final configuration consists of a top layer of large Si crystalline plates on a composite layer of Au and polysilicon

where the Au is distributed in a network of spikes and sublayers within the polysilicon layer.

This work[1a] investigates quantitatively the growth kinetics of the Si crystals by *in situ* sheet resistance measurements[4] and scanning electron microscopy (SEM) measurements.

4.2 Experimental

Polysilicon thin films 4500 Å thick were deposited via low-pressure chemical-vapor-deposition (LPCVD) process at 620°C, on thermally oxidized single crystal Si wafers. TEM cross-sections and x-ray diffraction (XRD) of the these films indicated that the grains were columnar and had [110] fiber texture.[1]

A total thickness of 2500 Å of Au was deposited onto the polysilicon films via resistive thermal evaporation with base pressure of $5x10^{-6}$ Torr. Samples were subsequently annealed in a vacuum furnace at a pressure of $1x10^{-7}$ Torr. The temperature control had a precision of +/- 0.5 °C.

Sheet resistance measurements were obtained *in situ* via a Van der Pauw type arrangement of 4 molybdenum spring loaded probes. A JEOL™ 35 scanning electron microscope (SEM) was used to obtain images of the Si crystals, and quantitative dimensions of the crystals were obtained via image processing techniques. Rutherford Backscattering Spectroscopy (RBS) was used to determine the thickness of the Si and Au films.

4.3 Sheet Resistance Measurements

When Au/polysilicon bilayers are isothermally annealed (Fig. 4.1), the sheet resistance R(t) of the sample increases with time. In order to relate the changes in resistance to the kinetic process of the reaction, we adopt a physical model which represents the sample as two regions: the top region, outlined by the original Au film, and the bottom region, framed by the original polysilicon film. Initially, the top region contains only Au; the volume fraction of Si in this region is zero. As the reaction proceeds and the Au is replaced by the formation of isolated Si grains, the layer becomes progressively more resistive. The bottom layer, which was initially electrically semiconducting, becomes more conductive with the anneal, as the displaced Au penetrates the polysilicon, forming a complex, conductive network of vertical spikes and sublayers. Since Au and Si are immiscible at these temperatures, the Au and Si remain separate. The redistribution changes the geometry of the effective conductive path which results in the increase of the overall resistance.

The reacted system is quantitatively related to the measured resistance by modelling the top and bottom regions of the sample as two parallel resistors. The conductance of each region is assumed to be proportional to the amount of Au in each region. By coupling the conductance of the two regions via conservation of Au, we can relate the volume fraction X_R of Si crystals in the top Au layer with the measured resistance R(t),

$$X_{R(t)} = [\,(R_o - R_{(t)}) / (R_o - R_F)\,]\, R_F/R_{(t)}\,, \qquad (4.1)$$

in terms of the initial (R_o), and final (R_F) values of resistance.

Equation (4.1) can be applied directly for analyzing a layer-by-layer

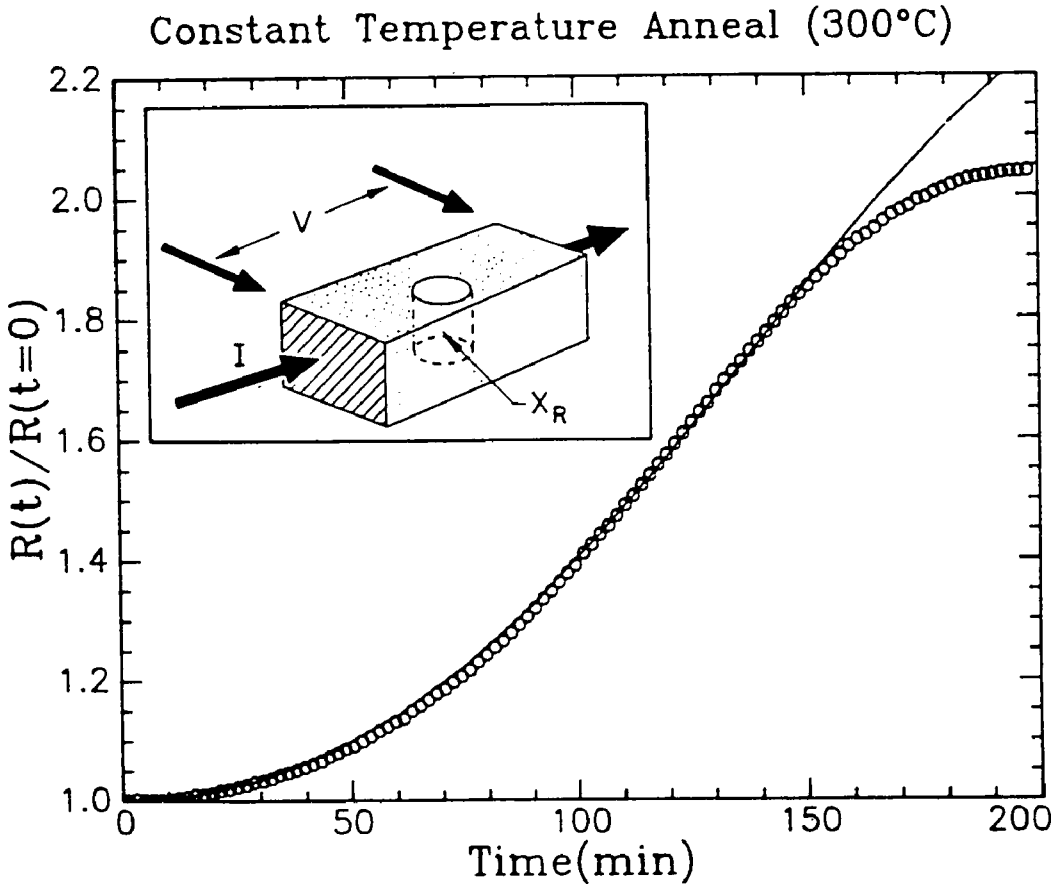

Figure 4.1 Normalized resistance measured *in situ* during 300°C isothermal anneal. Solid line represents model (Eqs. 4.1, 4.2 & 4.3) with n=2.0, R_o/R_F = 2.5, and τ = 87.7 s. The diagram (inserted) represents effective model of the measurement.

growth process[5] where $X_R(t)$ would be proportional to the thickness of the growing layer. However, Eq. (4.1) must be modified in the latter stages of the reaction, in systems where crystal growth is influenced by the impingement of adjacent crystals and percolation prevails. The transformed fraction $X_{R'}$ of the reaction which includes impingement is related to the actual volume (area) fraction X_R by using the Avrami equation[6],

$$X_R = 1-\exp(-X_{R'}) \quad . \tag{4.2}$$

At the initial stage of the reaction, where there is no impingement, $X_{R'}$ is small so that $X_R \approx X_{R'}$.

Equations (4.1) and (4.2) were applied to the resistance data in order to obtain the time dependence of the transformed crystal volume fraction $X_{R'}$ in the initial stage. The parameter R_F was used as a fitting parameter in Eq (4.1), because the final resistance of the system was not well defined, since the resistance continued to change even after the reaction was completed due to further redistribution of the Au in the underlying layer of crystal platelets. By plotting the resistance data (Fig. 4.1) in the form of $\ln(X_{R'})$ vs. $\ln(t)$ (Fig. 4.2), we observe the general relationship

$$X_{R'} = 1/2(t/\tau)^n. \tag{4.3}$$

where τ is a time-independent constant. A value of $n \approx 2.1$ was obtained from the slope of the curve, indicating that the reaction proceeds with approximately a t^2 dependence. A comparison of the calculated time dependence using Eq. (4.1) ($n=2$ and $R_F/R_0 = 2.5$) are compared with original data in Fig. 4.1 and shows good agreement through ≈80% of the reaction.

The parameter n is the mode parameter in the reaction process; it can have various values depending on the rate-limiting process(es) in the system. Tables generated by theoretical models have yielded various

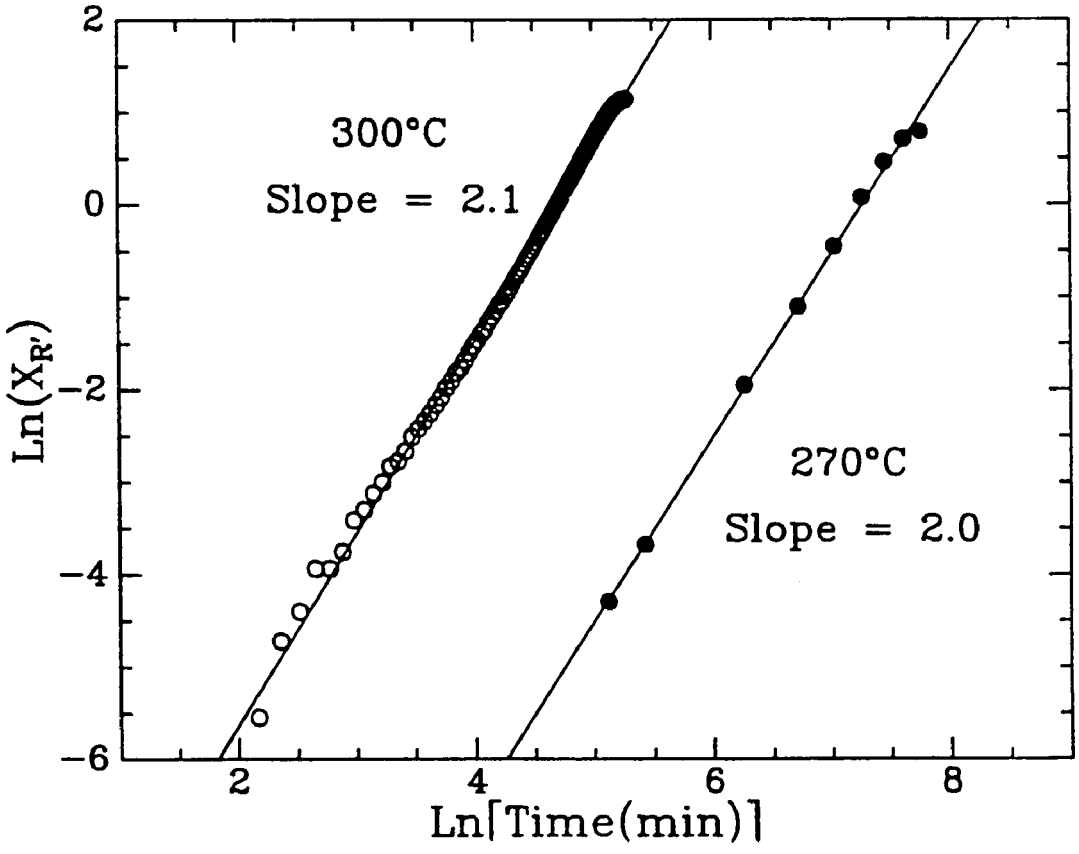

Figure 4.2 Resistance data from Fig. 1 reduced to a from which accounts for crystal impingement. The plot $\ln(X_{R'})$ vs. ln (t) indicates the relationship $X_{R'} \propto t^n$ where n=2.1 is the slope.

values of n for particular combinations of nucleation and growth processes[7-9]. For example, in the case of a constant number of spheres growing in a 3-dimensional manner, where the interface (surface of the sphere) limits the rate of growth, the time dependence would be t^3 (n=3). In the 2-dimensional case, where plates are growing, the time dependence would be t^2 (n=2). However, we cannot uniquely identify the rate controlling process based solely on the value of n, since multiple processes (i.e., growth and nucleation) may individually control the rate of reaction. Although the origin of crystals is due to grain growth and not to nucleation, this does not preclude the possibility of the number of grains changing during the anneal. In order to separate the time-dependent effects of growth from the number of crystals, we measured the number and volume (area) of the crystals using SEM.

4.4 SEM Measurements

The growth process of Si crystals was measured directly via SEM analysis. The Si crystals in the top layer were easily observed by SEM, appearing as dark patches in the film. The data presented in this section were obtained from different samples from the same substrate. Each sample was isothermally annealed only once, at a specific temperature (T) for a given anneal time (t). The number of crystals, as well as their size, were measured using the image-processing capabilities of the SEM system. The average crystal size was determined by dividing the fraction of the area covered by crystals by the total number of crystals. Data collection was limited to the first 30% of the reaction so as to avoid significant crystal

impingement. During the first 30% of the reaction, the crystals were observed to grow independently of each other.

SEM micrographs (shown in Fig. 4.3) were obtained from samples annealed isothermally at 270°C and 290°C for various anneal times. We first investigate the number of crystals during the anneal. The average number (N) of crystals vs anneal time is plotted (Fig. 4.4) for two (270°C and 290°C) anneals. The data indicate that at a given temperature the number of crystals is fixed at the beginning of the reaction and does not appreciably change during the anneal. However, the number of crystals does depend on temperature, N(T). The average number of crystals during the 290°C anneal ($\approx 0.07/\mu m^2$) is three times higher than the number observed during the 270°C anneal ($\approx 0.02/\mu m^2$).

Although the number of crystals does not change during the anneal, the crystal area increases significantly with time. The average crystal area is plotted as a function of time (Fig. 4.5) for anneals at 270°C and 290°C . The data indicates that at the early stages of the reaction (<50%) there is a linear relationship between the square root of the crystal area (A) and time t

$$A^{1/2} = \pi^{1/2} \, v \, t \, . \qquad (4.4)$$

The factor v, referred to as the linear growth rate (velocity), is constant, and is obtained by measuring the slope of the $A^{1/2}$ vs t curve. The parameter v(T) does depend on the anneal temperature, increasing from 0.2 Å/sec at 270°C to 1.25 Å/sec at 290°C.

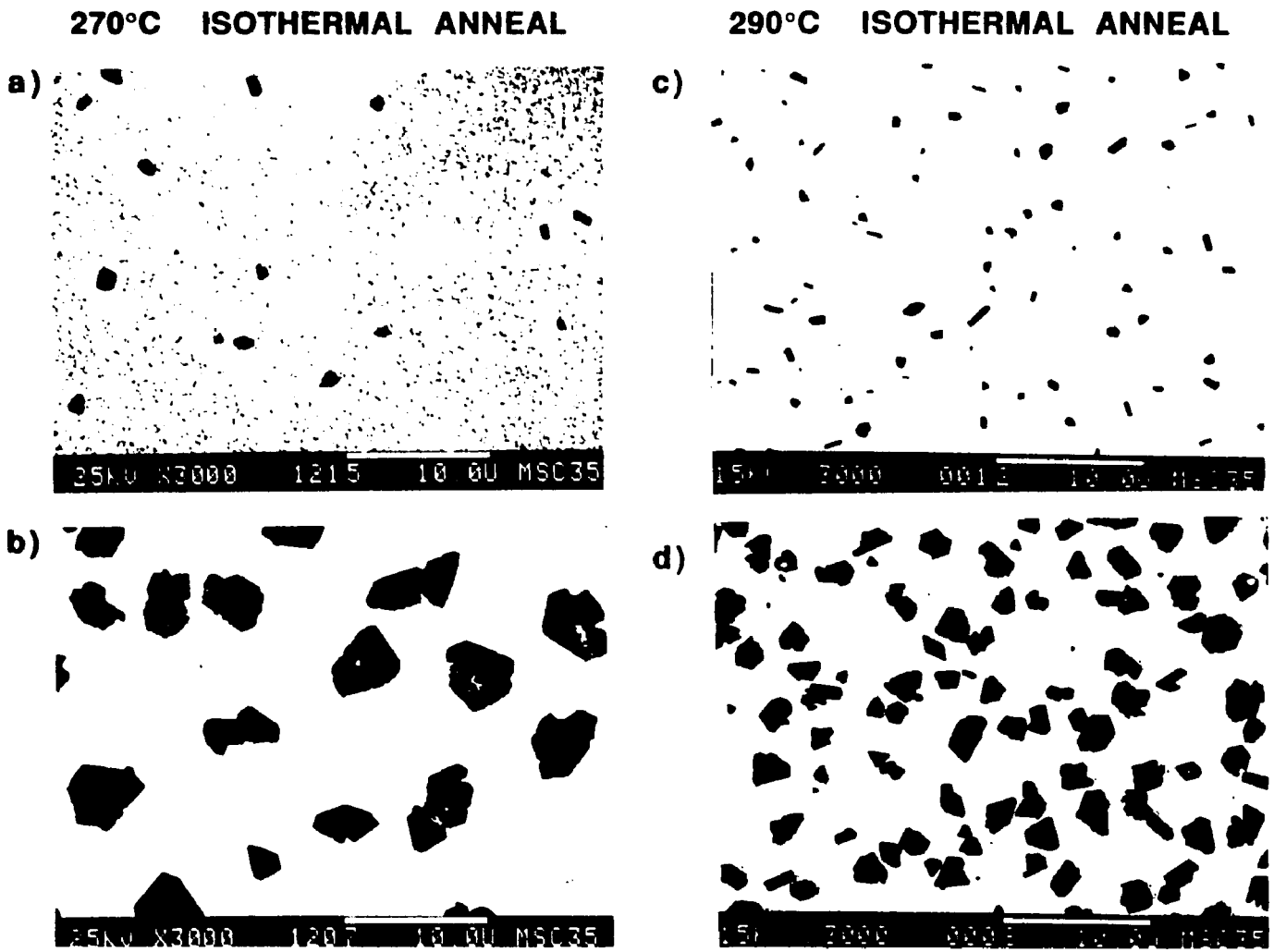

Figure 4.3 SEM micrographs of four different samples annealed at (a) 270°C (380 min), (b) 270°C (1900 min), (c) 290°C (76 min), & (d) 290°C (196 min).

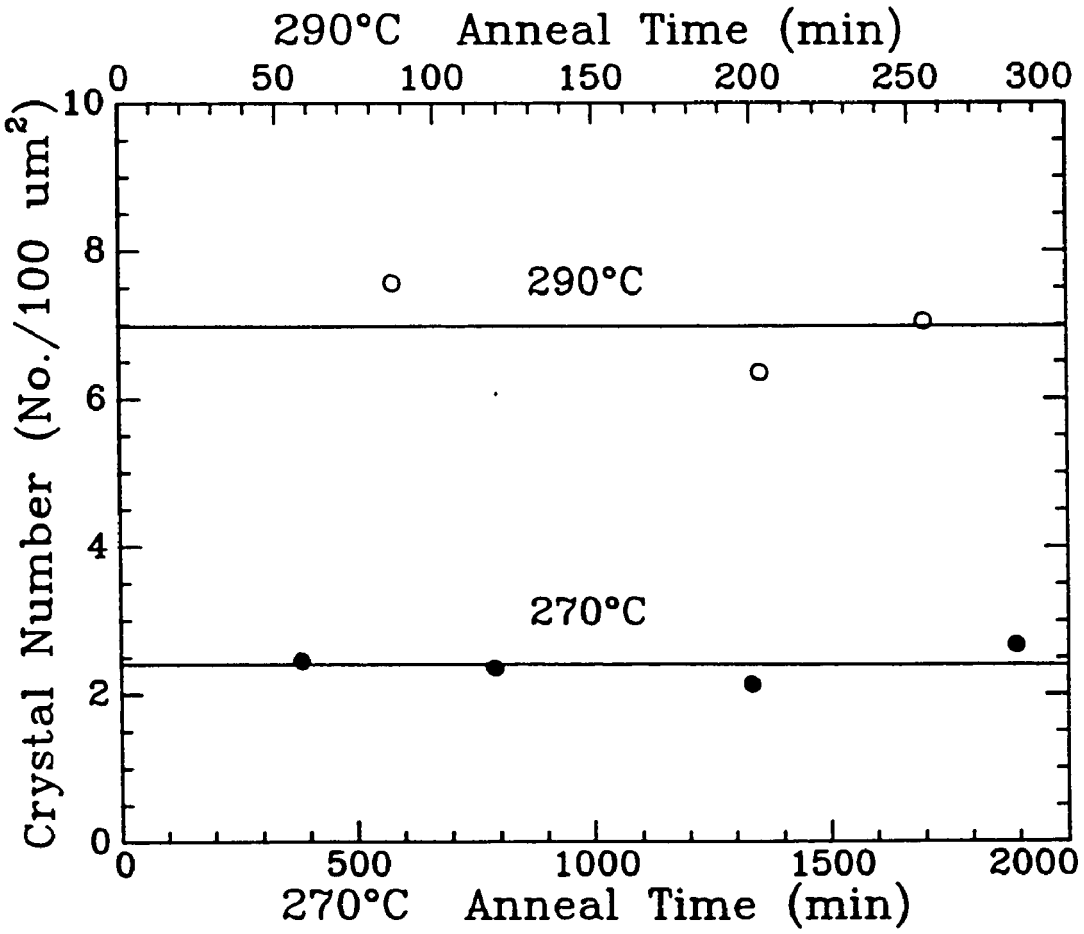

Figure 4.4 Number of crystals per unit area (N) as a function of anneal time and temperature. The 290°C anneal is plotted vs time on the top axis and the 270°C anneal is vs time on the bottom axis.

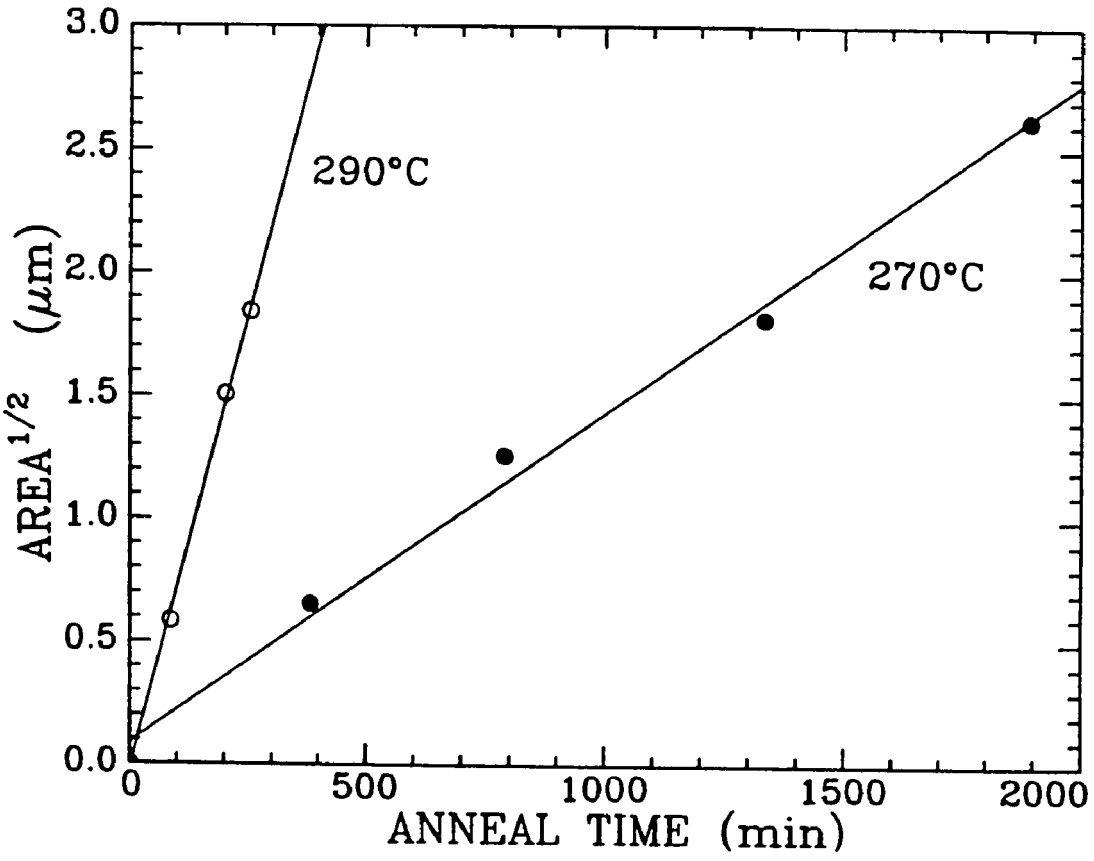

Figure 4.5 The growth rate is plotted as the square root of the average crystal area ($A^{1/2}$) vs the anneal time at two (270°C and 290°C) temperatures.

4.5 Temperature dependence of growth rate v and the number of crystals N

To determine the temperature dependence of N(T) and v(T), the crystal area and the number of crystals were measured over a range of temperatures. The data shown in Fig. 4.6a and Fig. 4.6b indicate that both parameters follow the Arrhenius-type relation; $N(T) = N_o e^{-E_N/kT}$ and $v = v_o e^{-E_v/kT}$, where N_o and v_o are constants. Two separate activation energies (E_N =1.0 eV and E_v =1.9 eV) were experimentally determined from the data. The activation energy E_N is associated with the number of crystals at a given temperature and E_v is associated with the crystal-growth rate at a given temperature.

Having analyzed the reaction in terms of the individual process components, the crystal number (N) and growth rate (v), we can now construct an expression for the reaction. The total area fraction X_{SEM} of the surface covered by the crystals at any time and temperature as determined from SEM data can be expressed as the product of the number (N) of the crystals per unit area and the average area (A) per crystal:

$$X_{SEM} \equiv N(T)\, A(T,t)\,. \tag{4.5}$$

By using the experimentally determined relationships between the parameters, X_{SEM} can be expressed explicitly in terms of time and temperature as

$$X_{SEM}(T,t) = \pi\, N_o\, v_o^{\,2}\; e^{-(E_N+2E_v)/kT}\; t^2\,. \tag{4.6}$$

The results obtained from the SEM data can be summarized as follows. The accumulative process of replacing the Au layer with Si crystals is a product of two separate factors: the number of crystals, which is independent

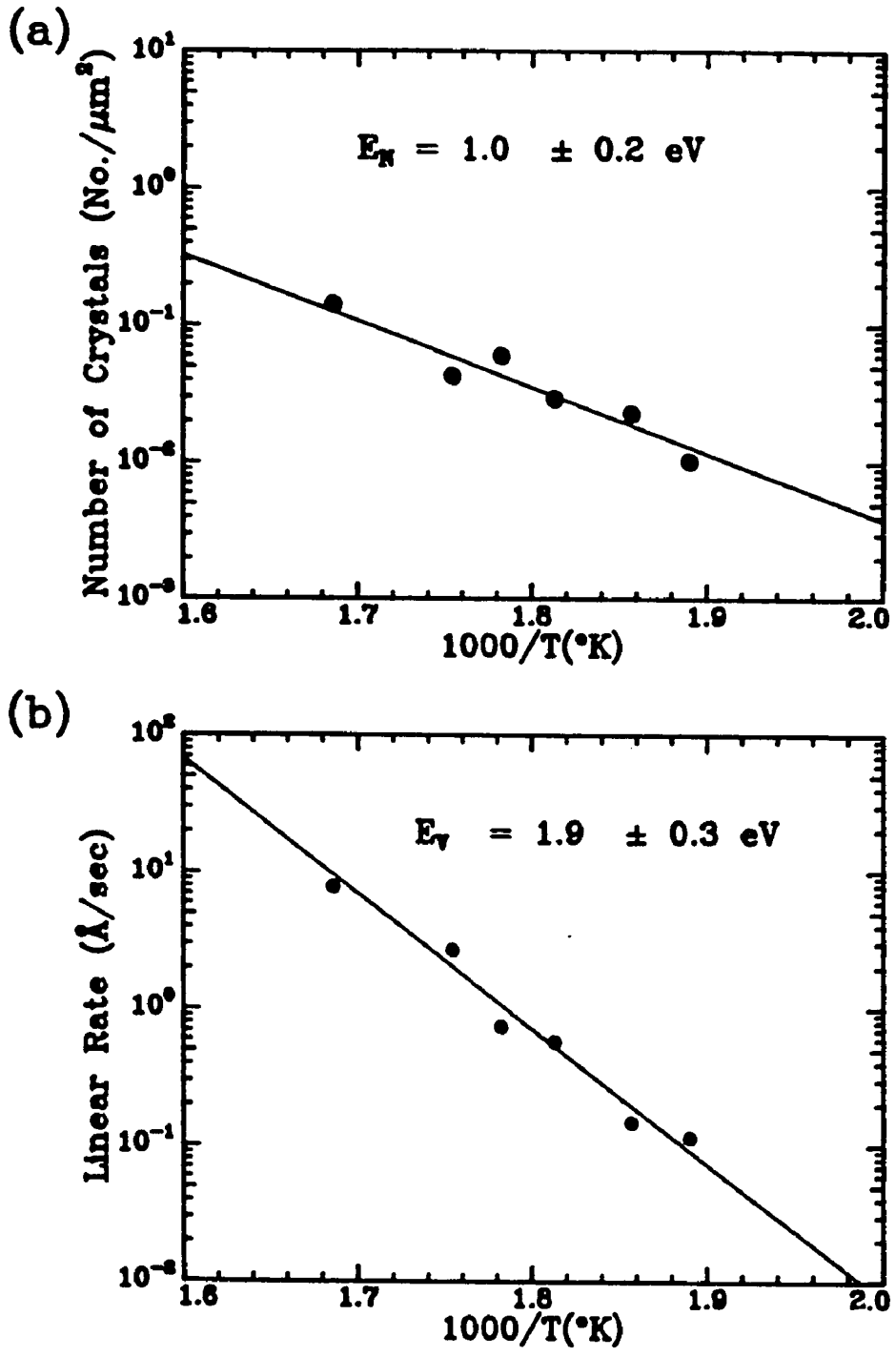

Figure 4.6 (a) The number of crystals per unit area (N), and (b) the linear rate of growth (v) are plotted vs 1000/T°(K).

of time but thermally activated, and the crystal-growth process, which has a given ($A^{1/2} = \pi^{1/2}$ v t) time dependence where the rate constant v is time independent but thermally activated.

4.6 Comparison of Resistance and SEM Results

We compare here the results obtained from the SEM data with the resistance data. This is accomplished by utilizing a parameter τ, which can be related to both resistance and SEM measurements. The parameter τ is defined as the time of anneal at which the reaction is 50% completed. For the resistance measurements, τ is extracted directly from the data with the requirement that $X_R \approx 0.5$. In the case of the SEM data, τ_{SEM} is calculated from the SEM data using the relation $\tau_{SEM} = (2\pi Nv^2)^{1/2}$ which is derived from Eqs. (4.4) and (4.5). with the condition that $X_{SEM}(t=\tau) = 1/2$. The values for τ_{SEM} and τ_R obtained from both SEM and resistance data are plotted together in Fig. 4.7, and show good agreement. This confirms the claim that the methods, although independent of each other, are equivalent [$X_{SEM}(\tau) \approx X_R(\tau)$]. The difference is that the SEM measurement is able to separate the overall process of transformation into its components.

The resistance and SEM data shown in Fig. 4.7 correspond to an Arrhenius plot with a characteristic activation energy. Typically, the characteristic activation energy of a system is analysed via an Arrhenius plot (Fig. 4.7), by measuring the slope of the data and using the general phenomenological relation

$$\tau = \tau_o e^{E_\tau/kT} \qquad (4.7)$$

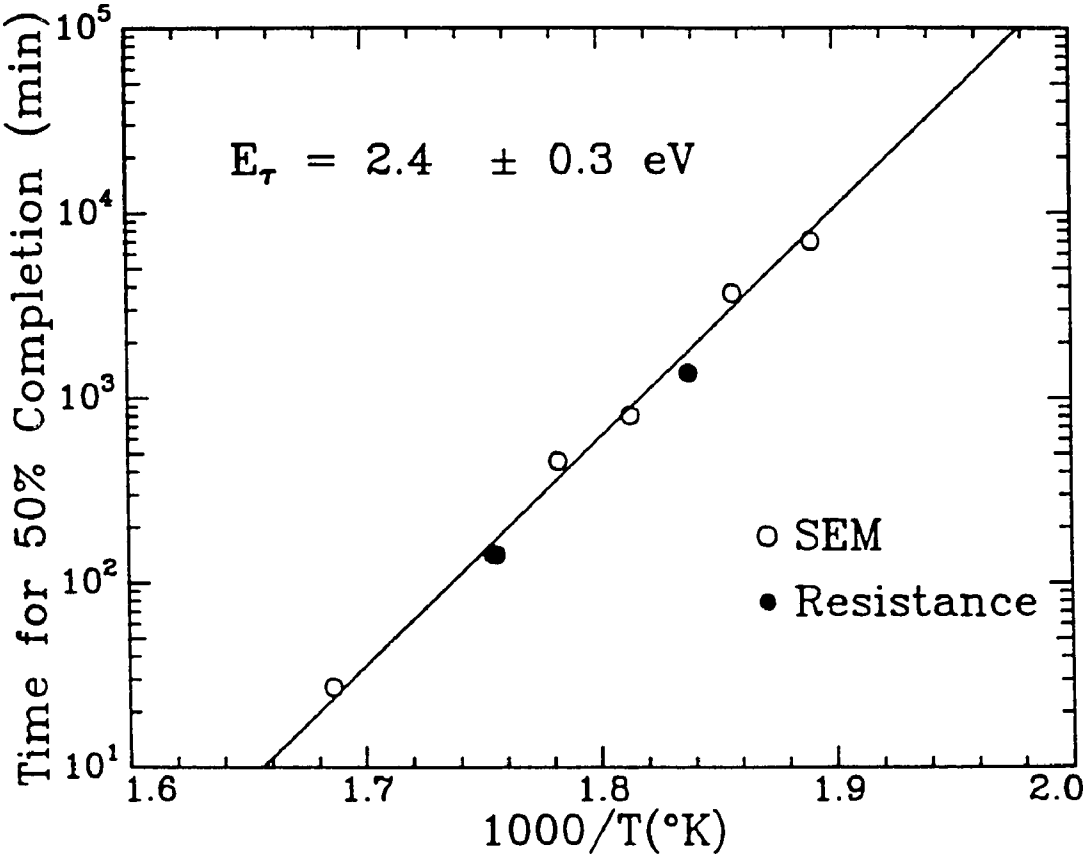

Figure 4.7 Values of t vs 1000/T(°K) from resistance (•) and SEM (o) data are compared. The parameter t is the time it takes for the reaction to proceed to 50 % of completion.

where τ_o is temperature independent. From the analysis of the data, we obtain values of $E_{\tau_{SEM}} \approx E_{\tau_R} \approx 2.4$ eV for the activation energies measured by two the independent methods. This specific activation energy represents the activation energy of the entire process.

4.6 Comparison of activation energies.

It is useful to relate the phenomenological parameter $E_{\tau_{SEM}}$ with the specific process which determines the number of crystals (E_N) and the process of grain growth (E_V). Since the activation energy $E_{\tau_{SEM}}$ was obtained from the same set of data as the values E_N and E_v, it is not surprising that the parameters are dependent on one another. The relationship between the activation energies can derived by evaluating Eq. (4.6), and setting $X_{SEM} = 1/2$ at time $t = \tau_{SEM}$. :

$$\tau_{SEM} = (2\pi N_o v_o^2)^{-1/2} \exp[-(E_N+2E_V)/2kT] . \qquad (4.8)$$

Given that the phenomenological relation is defined by

$\tau_{SEM} = \tau_{o_{SEM}} \exp(E_{\tau_{SEM}}/kT)$, the expression in Eq. (4.8) can be further reduced to the the following equation:

$$E_{\tau_{SEM}} = E_N/2 + E_v - kT/2 \ln(2\pi N_o v_o^2 \tau_{oSEM}^2) . \qquad (4.9)$$

Since all of the parameters $E_{\tau_{SEM}}$, E_N, E_v, N_o, v_o, and τ_{oSEM} are temperature independent, it can be shown that the term kT/2 ln() in Eq. (4.9) will be zero, and therefore

$$E_{\tau_{SEM}} = E_N/2 + E_v \quad . \qquad (4.10)$$

To confirm this result, values for E_N and E_v have been compared with E_τ ($E_{\tau_{SEM}} = (1.0/2 + 1.9)$ eV = 2.4 eV) and again show good agreement.

The factor 2 in Eq. (4.10) is a consequence of the growth mode of the system. In general, given a reaction of interface-limited-growth with instantaneous nucleation (or, as in our case, a constant time-independent number of crystals), the factor will equal the number of degrees of freedom of growth. This factor would be equal to 3 if the crystals were growing in three dimensions, and would be one if the crystals were limited to one dimensional growth.

4.7 Effects of Various Polysilicon Substrates

The rates of the reaction for three separate polysilicon substrates (LPCVD 620°C) are plotted in Fig. 4.8 in terms of the parameter τ. The data show that the reaction rate varies considerably, by a factor of ≈ 50, from one substrate to another, although the activation energies are comparable (E_τ = 2.13, 2.21 & 2.38 eV). It was determined from several measurements that the variation in reaction rates is mainly due to variations in the polysilicon deposition: substrates within a particular deposition batch gave similar reaction rates. On the other hand, the variation in the Au deposition process did not produce significant variations in the reaction rate.

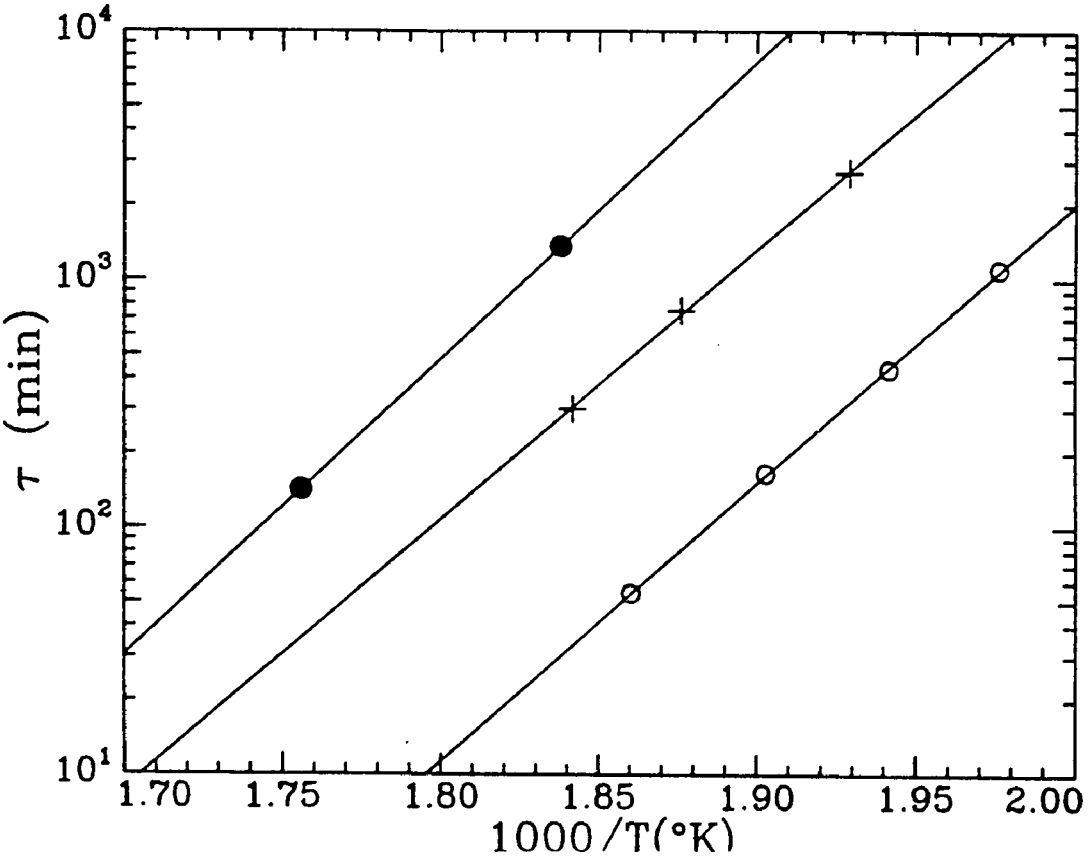

Figure 4.8 The reaction rate in terms of t ($X_R(t)=1/2$) is plotted vs 1000/T(°K) for three different polysilicon substrates.

4.8 Discussion

The growth of Si crystals is a thermally activated process, with the rate of the total transformation proportional to $\exp(E_t/kT)$. Because the crystals are large and separated from each other, it is possible to describe the total transformation as a product of two processes which control the the number of crystals and their growth rate. This discussion analyses the time and temperature dependence of each process and relates the individual activation energy (E_v and E_N) to basic physical mechanisms.

Individual Si crystals grow at a rate which has an activation energy of E_v = 1.9 eV. The number of growing crystals is fixed at the beginning of the reaction and remains the same throughout the anneal, but the number of crystals depends on the temperature of the isothermal anneal, having an activation energy $E_N \approx$ 1.0 eV. The relationship among these activation energies is given as $E_t = E_v + E_N/2$

The rate of growth of the crystal area was established by experimental data as $A^{1/2} = \pi^{1/2}\ v\ t$. If the crystals had the shape of circular disks, the parameter v (μm/min), would be easily interpreted as a constant growth velocity of the circumference of the crystal. Since the crystals in this study have faceted shapes, a simple relationship between v and the growth rate of the edges of the crystal cannot be directly established. The physical meaning of v is assumed to be an average velocity of all the edges of the crystal, each growing at a constant rate.

The condition of a constant growth rate that is independent of crystal size and shape is consistent with an interface-limited growth process. Therefore we conclude from this result that the growth of the crystal is limited

by the interface (Au/c-Si) and is not limited by the diffusion of Si through the Au.

Since the number of crystals does not change during the reaction, we can further evaluate the reaction-rate parameter n [(Eq. (4.3)] obtained from the resistance data. From Dormeus[7] the factor n would have values of 1/2 (plate-shaped crystals) or 3/2 (spherical-shaped crystals) in a diffusion-limited growth mode. If the system were controlled by an interface-limiting process, the factor n would have a value of 2 (plate-shaped crystals) or 3 (spherical-shaped crystals). The measured value of n in this study was 2.1, which agrees with previous analysis in that the reaction is controlled by the interface-limited growth of plate-shaped crystals This localized interface process is speculated to be a process of fitting an atom to the growing interface of the crystal. The activation energy $E_v \approx 1.9$ eV is associated with growing Au/crystal Si interface. We expect the energy E_v to be 2 eV or slightly higher since it should be close to the energy needed to add or remove a Si atom from a low index surface of Si crystal[10].

Although diffusion does not limit the growth rate of the crystals, it does play an key role in determining the distance between the crystals, and will be discussed later.

An interesting result for Au/polysilicon is the unusually large size of the Si crystals. Since the size of the crystals is inversely proportional to the number of the crystals N, it is useful to discuss those factors that may control the value N. A key result of this investigation is that the number of growing crystal is fixed at the initial stage of the reaction and is time independent. The origin of these crystals has been investigated[1], and it was concluded that each crystal is the result of the growth of an already existing grain

located at the initial Au/polysilicon interface which grows in a 3-D manner until impinging the top surface, and then grows in a 2-D manner radially to form two-dimensional platelike crystals. The growing Si crystal displaces the Au. Given the wide initial distribution of grain sizes[2] at the interface, only the larger grains are expected to grow (Ostwald ripening). These grains grow at the expense of the smaller grains. The relationship between the driving force for growth and the size of the grain is a simplification of the *Thomson-Freundlick* relation, which relates the driving force in the system to the radius of curvature of the particle. Since the polysilicon is an accumulation of columnar grains with a wide variation of diameters, we assume the simple relationship that the size/diameter of the grain is directly (inversely) related (on the average) to the curvature of the exposed surface.

Ideally, there would be only one largest grain for the entire sample, and this grain would grow at the expense of all other grains, which dissolve into the Au at a rate prorated according to their size. But the diffusivity of Si in Au is finite and thus restricts the transport of Si from distances far away from the growing crystal. The area from which the crystal draws the Si is limited to the immediate vicinity of the crystal. The extent of this affected area depends on two factors: the local dissolution rate of the polysilicon crystals and the diffusion of Si through Au. The size of this local region determines the final size/number of crystals.

Since the diffusivity of Si in Au is finite there will be a concentration gradient of Si in the Au perpendicular to the growing interface. The dissolution rate of the the polysilicon grains near the growing crystal will be higher than those far away from the crystal. This was verified from TEM data[1], which clearly shows that more of the polysilicon grains were dissolved

in the region near the crystal. A schematic diagram of this process is shown in Fig. 4.9.

A quantitative analysis of the dissolution and diffusion of Si to the crystal is treated in the appendix A. From this analysis we obtain an expression for the radius (L) of the affected region,

$$L^2 \propto D/B \quad , \tag{4.11}$$

in terms of the diffusion coefficient (D) of Si in Au and the average dissolution rate (B) of the polysilicon grains. This parameter L sets the initial boundaries of the affected area at the early stages (<5%) of the reaction. At the latter stages of the reaction the affected regions of the crystals will overlap, suppressing to an even greater extent the growth of other grains in the region between crystals. Therefore it is the initial value of L that determines the distance between the crystals (see Fig 4.9) and, consequently, the number of crystals per unit area N, since

$$\pi L^2 \propto 1/N \ = \lambda_N D/B \ , \tag{4.12}$$

where λ_N is a constant. The value for N is expected to be constant throughout the anneal, as is experimentally observed.

Assuming a simple dependence of $B = \lambda_B \exp(-E_B/kT)$ and $D = \lambda_D \exp(-E_D/kT)$ on temperature T where λ_B and λ_D are constants, it follows from Eq. (4.11) that

$$N_o \exp(-E_N/kT) = (\lambda_B/\lambda_N\lambda_D) \exp(-E_B/kT) / \exp(-E_D/kT). \tag{4.13}$$

Since N_o, λ_B, λ_N, λ_D, E_N ,E_B and E_D are all assumed to be temperature independent it can be shown that $1 = \lambda_N\lambda_D N_o / \lambda_B$ and we can set the coefficients of T (on each side of the equation) equal to each other,

$$E_N = E_B - E_D \, . \tag{4.14}$$

Consider the dissolution factor B, the rate at which Si atoms are

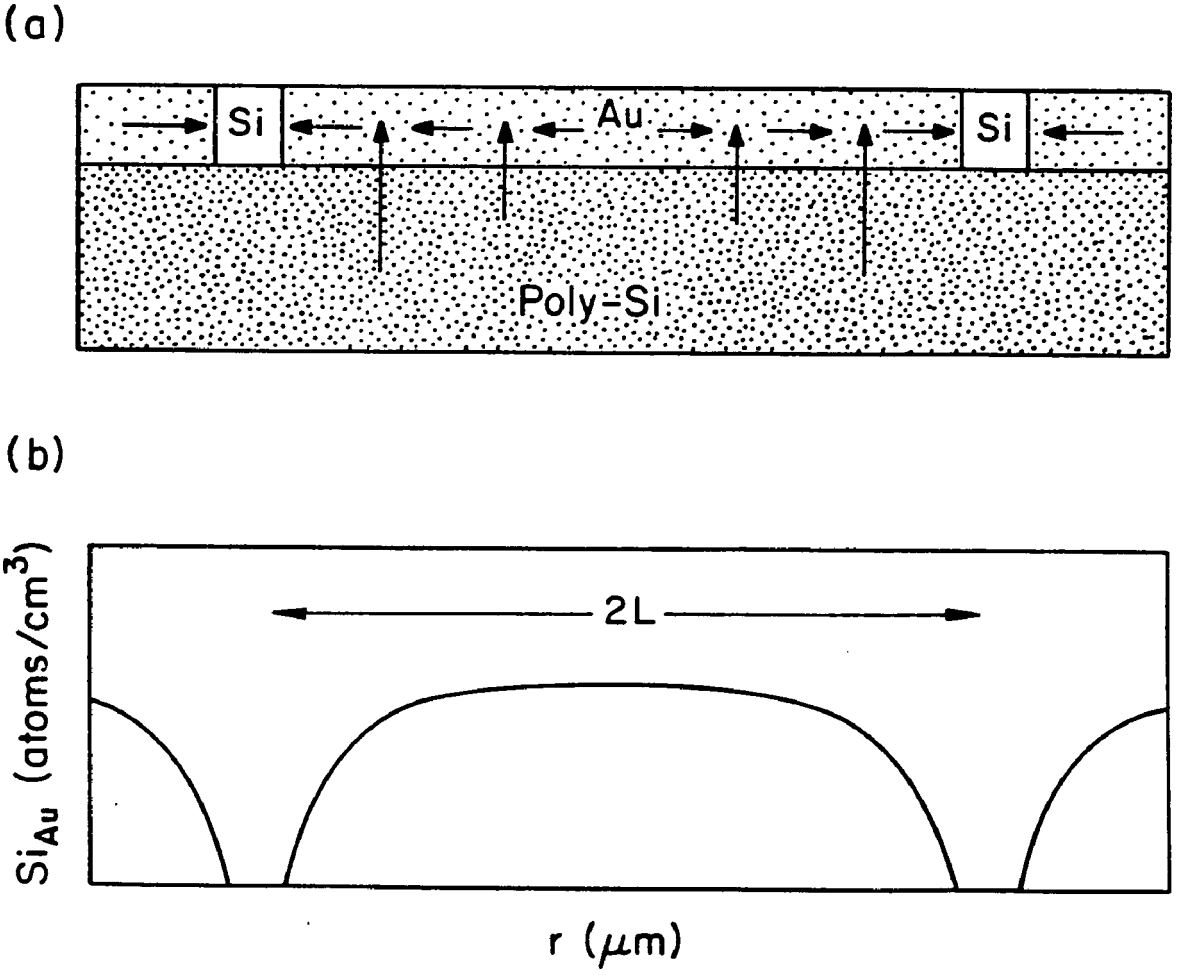

Figure 4.9 (a) A diagram of the two dimensional model describing the dissolution of Si from the polysilicon layer and the diffusion of Si toward the crystals, and (b) the Si concentration profile C(r) within the Au.

removed from the small-grain Si. For a given crystal at equilibrium, the dissolution rate will equal the growing rate. It can also be shown that for the same crystal the activation energy of the growth rate is equal to the activation energy of the dissolving rate. We argue that the activation energy of dissolution rate E_B of the small-grained crystals will be approximately equal to the activation energy of the growth rate of the large-grained crystal (c-Si), E_v, since the chemical potential difference of small vs. large Si grains is small (+/- 0.1 eV)[1]. Therefore we have

$$E_B \approx E_v \approx 1.9eV \qquad (4.15)$$

We could not obtain data regarding the activation energy E_D of Si in Au, so we assume a value[11] of $E_D \approx 0.8$ eV from the Al/Si system, which is another eutectic system that reacts with polysilicon in much the same way (Si crystal growth) as in the Au/Si system. Now we can evaluate the term E_N ($E_N = E_B - E_D \approx E_v - E_D \approx 1.1$ eV) and find good agreement with the measured value (E_N=1.0 eV).

At low temperatures the distance L_L will be large ($L^2 \propto \exp(1.1eV/kT)$) and the largest crystal will dominate, suppressing the growth of all other crystals within the region. At higher temperatures L_H will be smaller and the affected region will also be smaller, allowing additional grains outside of this region to grow. This process is diagrammed in Fig. 4.10.

We conclude from this analysis that the thermal activation energy (E_τ) for the total transformation process depends on two basic processes: the exchange of Si atoms from the Si surface (E_v) and the diffusion (E_D) of Si through Au. By combining Eq. (4.10,4.14 & 4.15), E_τ can be rewritten explicitly in terms of E_v and E_D.

$$E_\tau = 3/2\, E_v - 1/2\, E_D \qquad (4.16)$$

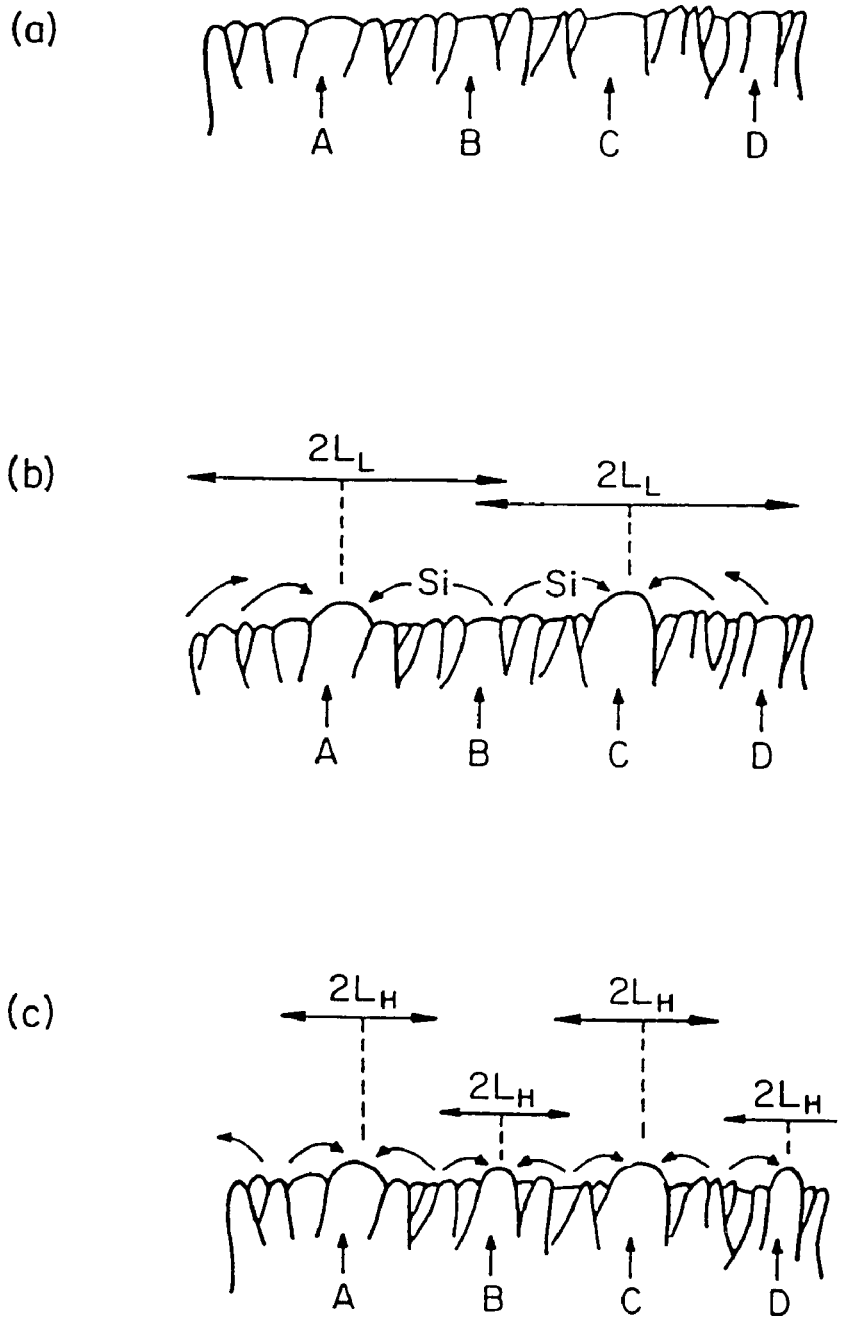

Figure 4.10 A diagram of the initial stages of crystal growth with (a) no thermal anneal, with (b) low temperature anneal (large diffusion length L_L), and (c) high temperature anneal (short diffusion length L_H) Note, only grains A & C grow at low temperatures while A,B,C &D grains grow at the higher temperature anneal.

Large differences in transformation rates, but comparable activation energies, were observed in a given set of polysilicon samples. It is speculated (and qualitatively supported via x-ray data) that the difference in reaction rate from sample to sample is due to differences in the average grain size. The rate of reaction at any given temperature would be expected to be strongly dependent on microstructure (i.e. average size of grains). The driving force for this reaction $\Delta\mu_{Si}$ depends strongly on particle size: The insensitivity of the activation energy to the type of polysilicon is expected since the basic mechanism (adding/removing Si atoms from Si and Si diffusion in Au) are insensitive to polysilicon microstructure.

4.9 Summary

This investigation characterizes the time and temperature depends of the formation of Si crystals during isothermal anneals of Au/polysilicon bilayers by using *in situ* resistance measurements and SEM analysis.

This reaction is controlled by two separate processes: the growth rate of the individual crystals, and the total number of growing crystals. Individual Si crystals grow with an interface-limited growth process within the Au layer at a constant linear growth rate (v) with an activation energy of E_v = 1.9 eV. The number of growing crystals is fixed at the beginning and remains the same throughout the anneal, but the number of crystals depends on the temperature of the isothermal anneal, having an activation energy $E_N \approx$ 1.0 eV. The relationship of these activation energies to the activation energy of the total reaction, E_t, is given as $E_t = E_N/2 + E_v$.

The number of crystals during an isothermal anneal is determined by the dissociation constant of the fine-grained polysilicon and the diffusion coefficient of Si in Au.

Further analysis of these separate processes show that they can be related to the more basic processes: the process of adding/removing Si atoms from a Si surface, and the diffusion of Si in Au. The activation energy of the overall process can be written as $E_t = 3/2\, E_v - 1/2\, E_D$.

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Chapter 5

Conformal growth of Si crystals and low temperature (300°C) Si homoepitaxy

5.1 Introduction

Thin film crystal growth via deposition (MBE,CVD, etc.) has been been characterized by many workers[1]. An alternative method of crystal growth is solid phase[2] recrystallization. Lateral solid phase crystal growth is of current interest because of the implication related to 3-dimensional electronic circuits[3].

In our earlier work[4,5] we observed the solid phase crystallization of large, two-dimensional Si crystals when bilayers of Au/polysilicon were annealed at temperatures below the eutectic (360°C). In this chapter, we look at two tangent issues related to the overall crystal growth process.

The first part of this chapter analyzes the Si crystal growth in the Au/polysilicon system when the initial support substrate has a patterned (stepped) topology. Unusual shapes of crystals occur in this system. Si crystals can apparently grow around corners (steps), yet maintain their single-crystallinity. TEM and SEM data are used to characterize shape and the quality of the crystals. The shape of the crystals conform to the topology of the Au layer, so it is referred to in this paper as the conformal growth process.

The second part of this chapter deals with homoepitaxial Si growth in

the Au/polysilicon system where the growing crystals have been seeded from the exposed (100) substrate. This is unusual because of the low temperature of the epitaxial growth (≈300°C).

5.2 Experimental - conformal crystal growth

Si wafers served as the supporting substrate for the experiment. Two types of non-flat samples were used. The first type consisted of the unpolished back side of a electronic grade Si wafer. The second type sample was fabricated by etching a pattern on the smooth side of the wafer using standard photolithographic and RIE methods.

All wafers underwent RCA cleaning process prior to thermally oxidation using which resulted in a ≈ 0.5 μm thickness of SiO_2. The fine grain polysilicon was deposited on the SiO2 layer by low pressure chemical vapor deposition (LPCVD) at 620°C with the resultant polysilicon thickness of ≈ 3000 Å. After cleaning the surface of the polysilicon with a buffered hydrofluoric acid solution, 3000 Å of Au was evaporated onto the polysilicon thin films at a pressure of $5x10^{-6}$ Torr.

Samples were then annealed at 290°C in a vacuum furnace with a base pressure of 10^{-7} Torr. This is below the Au-Si eutectic temperature of 360°C.

Cross-sectional TEM specimens were prepared by standard ion milling thinning techniques. JEOL™ 400Ex and 1200Ex electron microscopes were used to analyze the samples.

5.3 Results-conformal crystal growth

SEM micrographs shown in Fig. 5.1 were taken of samples after annealing and stripping the top layer of Au with a KI solution. Fig.5.1a shows single grain Si crystals situated on a layer of fine grain polysilicon. The initial substrate in this case was the smooth side of the Si substrate. Fig.5.1b shows a Si crystal formed on the rough side of a Si wafer where the topology of the substrate is not flat. It appears that the crystal originates at the bottom of the depression and grows laterally and scales the side wall of the depression. The growth apparently follows the contour of the substrate.

Crystals grown on the second type of (stepped) samples (patterned with RIE) were analysed with cross-sectional TEM. Fig. 5.2 shows dark field micrographs (2 beam condition) of the stepped region of the crystals where the Si crystal conforms to the topology of the step. The continuous pattern of the thickness fringes of the micrograph (Fig. 5.2a and Fig. 5.2b) show that the single crystals are continuous across the step and that the orientation of the crystal does not change going from one side of the step to the other. Selected area diffraction patterns were also obtained from the region on both sides of the step and confirm the continuity of crystallinity across the step. of the region. We deduce from this that crystal growth over the step is not interrupted due to twin or stacking fault defects.

Shown in Fig. 5.2c are two adjoined independent Si crystals which form the step. Note that only one of the crystals shows a bright contrast since the other crystal has a different orientation.

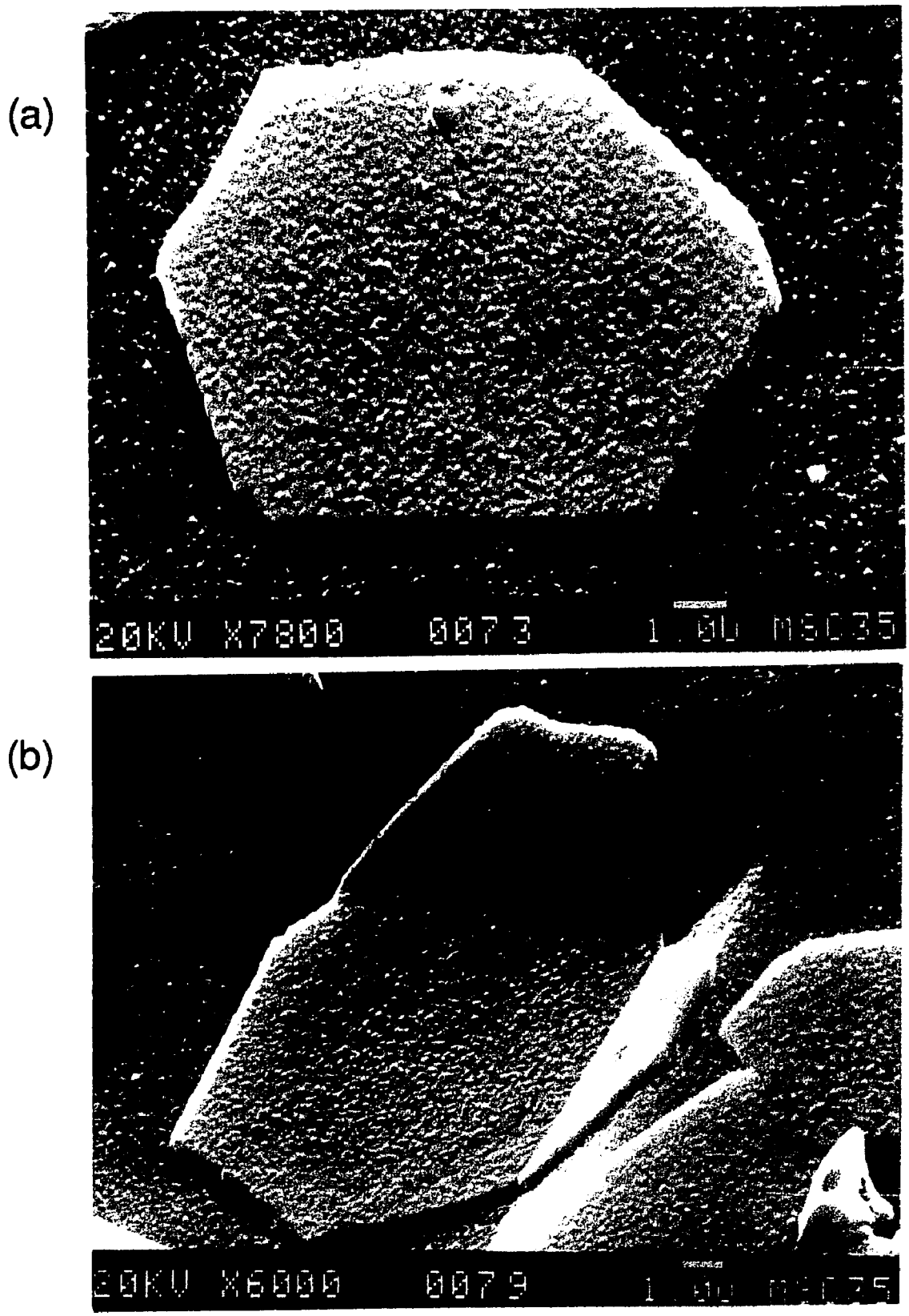


Figure 5.1 SEM micrograph of Si crystals on polysilicon of annealed Au/polysilicon/SiO2 sample after Au was selectively etched. Samples were fabricated on flat (a) and stepped (b) surface substrates. (from Ref. 5).

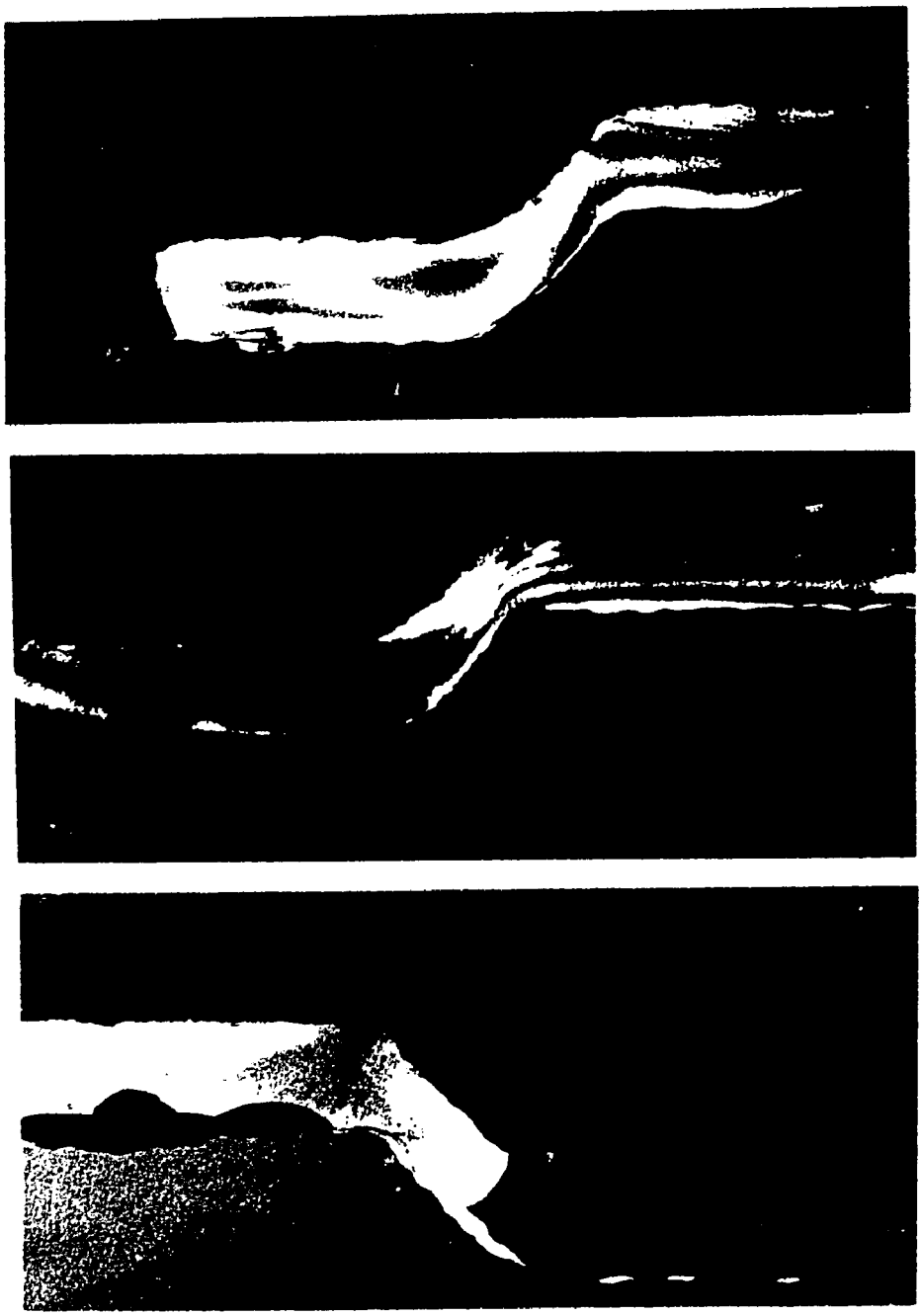


Figure 5.2 Dark field cross-section TEM micrographs (a) and (b)) of an annealed Au/polysilicon/SiO_2 sample showing the continuity of crystal growth across a step. Note the continuity of the bend contours, indicating a continuous single crystal. Two adjoined, independent Si crystals are shown in (c). Note that only one of the crystals shows bright contrast since the other crystal has a different orientation.

5.4 Discussion - conformal crystal growth

The two dimensional Si crystal growth on a stepped surface is apparently the same as the crystal growth on a flat surface. A purposed model of the growth sequence for the stepped surface is shown in Fig. 5.3. The cross-hatched marks in the crystal represent the equilibrium growth planes of the Si which are expected to be the (111) planes.

The shape of the Si crystal replicates the shape of the Au layer in a process which we refer to as conformal growth. An interesting and what unexpected feature of this phenomena is that the lateral growth is continuous at region near the step, where there is an abrupt change in the net direction of growth.

We seek to explain the apparent lack of sensitivity of crystal growth characteristics to changes in the direction of growth. To begin we note that the abruptness of the step is a matter of scale. Given the magnification at which the micrographs (Fig. 5.2) were taken, the step appears to be abrupt. But on a finer scale (e.g. the surface roughness (200 Å) of the Au layer) the patterned step appears as smooth, gradual, long-range perturbation of the original Au surface.

In deciding which scale is important in order to understand conformal growth, it is useful to discuss and speculate the mechanics of the growth process itself. It was concluded from earlier work[4] that the growth is interface-limited, localized at the crystal/Au interface at the growing face of the crystal[6]. We speculate that growth of the crystal face occurs via a layer-by-layer process, perhaps in monolayer increments. Each new monolayer of the crystal originates at a point (defect) on the crystal face (or edge) with subsequent completion (growth) of the monolayer. Given this method of

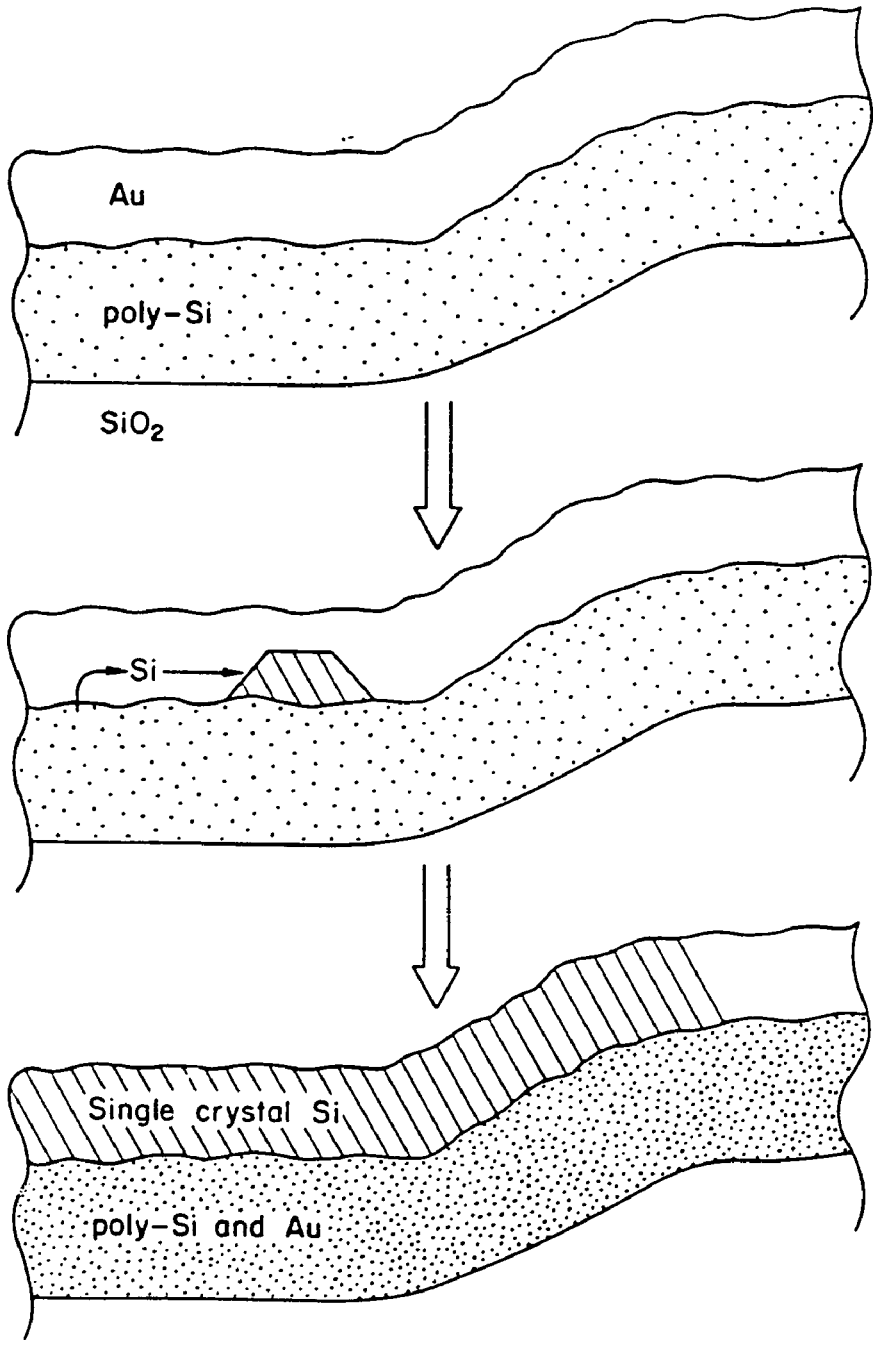


Figure 5.3 Model of the crystal growth sequence for a stepped surface. The cross-hatched marks in the crystal represent the (111) equilibrium growth planes.

growth and the scale at which it occurs (monolayer thickness ≈ 5 Å) , it is not surprising that the surface roughness or the long range shape of the Au layer (step) is not a critical factor for the growth and quality of the crystal.

The implications of this work (conformal growth) is that it provides for an additional degree of freedom in designing the shape of thin film crystals. Shapes which can not be fabricated with standard (MBE, etc.) methods could be generated using this conformal solid state recrystallization technique.. In principal, any shape of Si single crystal can be made given that a templet of Au can formed.

5.5 Experimental - homoepitaxial Si growth

The goal of the homoepitaxy experiments is to show that Si can grow if seeded on a Si substrate where the source of Si is the polysilicon layer. In order to connect the source (polysilicon layer) to the seed area (Si (100) substrate), special samples were fabricated. A schematic diagram shown in Fig. 5.4, describes the structure. (100) Si wafers are thermally oxidized which results in a ≈ 0.5 μm thickness of SiO_2. Fine grain polysilicon is then deposited on the SiO_2 layer by low pressure chemical vapor deposition (LPCVD) at 620°C with the resultant polysilicon thickness of ≈ 3000 Å. Selected areas of the polysilicon/SiO_2 regions are removed by first patterning with photoresist techniques and then an RIE etch. This exposes the (100) Si substrate. Then 3000 Å of Au is thermally deposited over the entire surface, thus providing a continuous diffusion path (Au) between the source(polysilicon) and the seed area (exposed Si substrate). These samples ,are then thermally annealed at ≈ 300 °C.

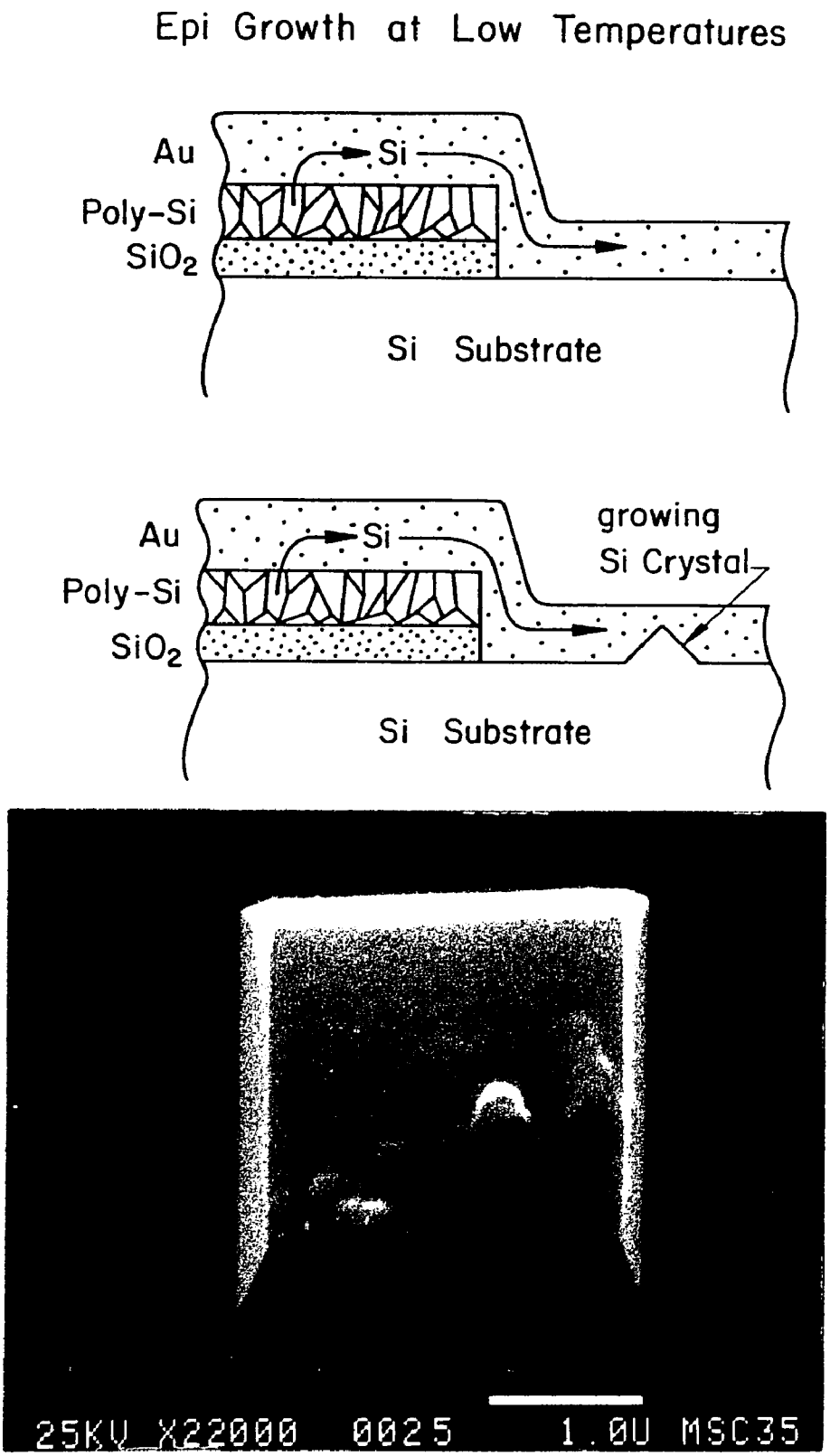


Figure 5.4 Epitaxial growth of Si, seeded on Si (100) substrate. The SEM micrograph shows a truncated pyramid crystal of Si on the Si substrate after the Au was removed by chemical etching.

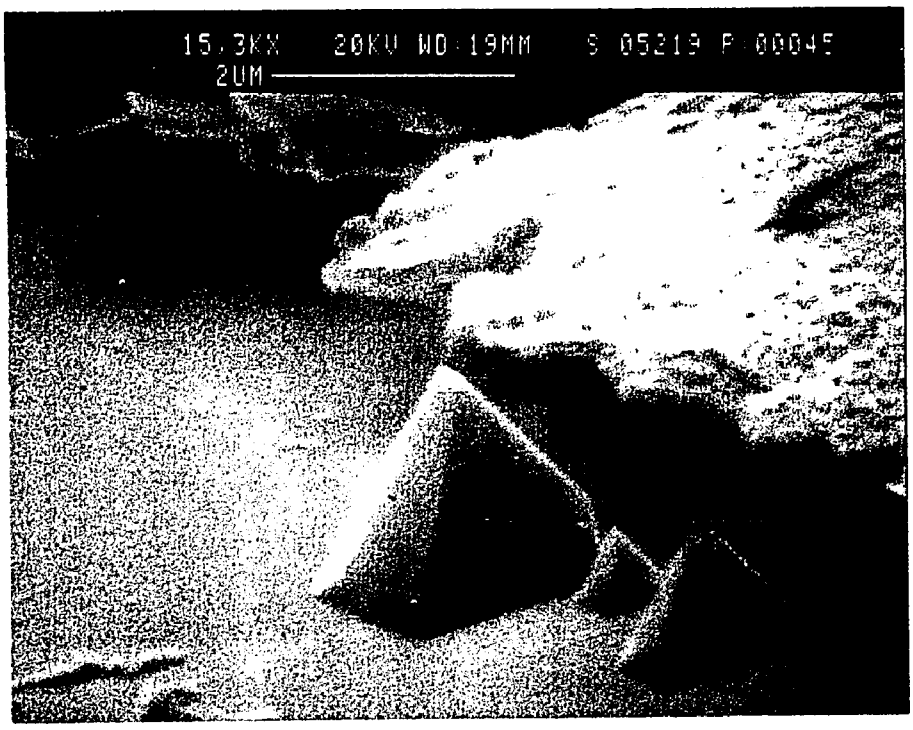
5.6 Results and discussions -homoepitaxial Si growth

Individual crystals begin to grow over the entire surface during thermal annealing of samples. As expected crystal growth occurs in the region containing the polysilicon in the same way as described in the previous chapters (3 & 4). But crystals also grow in the region where the Si substrate is exposed. These crystals, shown in Fig. 5.4, have the geometry of a truncated pyramid having (111) planes as faces. The height of the crystals will be equal to the thickness of the Au layer. For thick Au layers (>1 μm), larger untruncated pyramid structures are observed, as shown in Fig. 5.5.

Two growth characteristics of the homoepitaxial crystals which are of special interest is the origin and the resultant (pyramidal) shape of the crystals. First we must question the term "homoepitaxial" as applied in this case. These crystals seed on the (100) substrate at particular (partially random) places on the substrate. It is not a uniform planar process whereby monolayers of Si is epitaxially grown over the entire exposed Si substrate. The reason why the entire Si substrate surface is not involved in the growth process is not known. Perhaps the native oxide on the surface prevents initimate contact between the Au and the Si and therefore the crystals grow at particular pinholes through the native oxide. Or possibly the growth process initiates at particular point defects on the original Si surface. In any case it appears that the crystal initiates at small areas at the Si surface and then grows from the surface of the new crystal rather than at other areas at the original Si surface.

The pyramidal shape of the crystals can be qualitatively explained with the following argument. Given that the crystals are growing at equilibrium

(a)



(b)

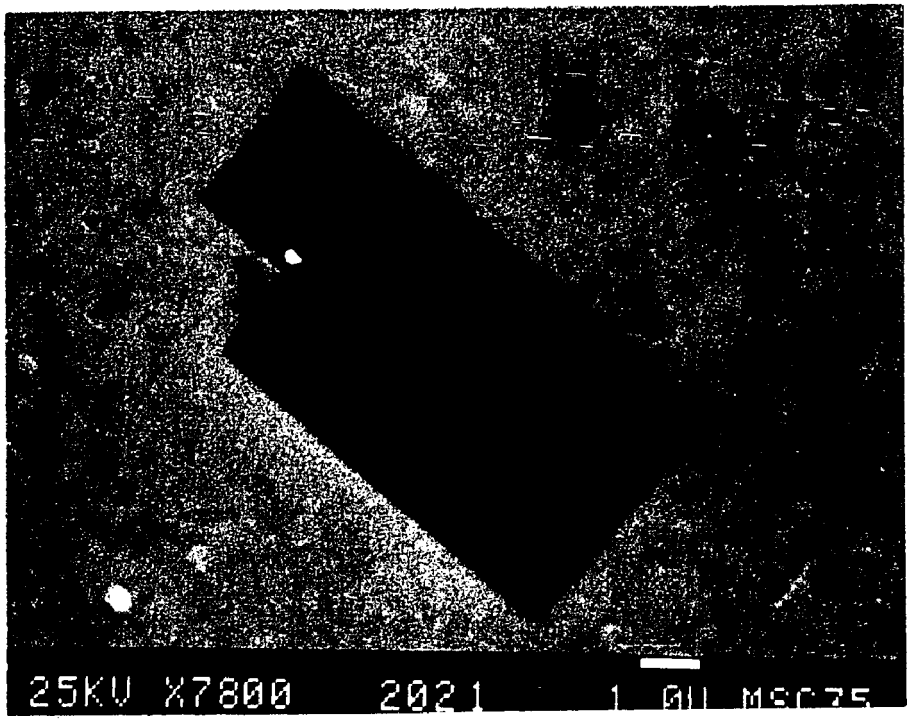


Figure 5.5 Homoepitaxial growth of Si on a (100) Si substrate. The height of the pyramidal crystals is equal to or less than the original Au layer. SEM micrographs in (a) were taken with the Au removed. The micrograph in 5.5(b) shows a planar view of a (dark contrast) large crystal (40 μm^2) where the Au has not been removed from the sample.

conditions and the growth is rate limited by a process at crystal face it seems reasonable that the resultant crystal faces which be the slowest growing (planes) faces of the crystal. It has been shown[7] in the case of Si that the rate of (homoepitaxial) regrowth of an amorphized Si layer grows slowest on a [111] substrate and fastest on a [100] substrate. Therefore it is expected that the crystal will assume a shape using only [111] surfaces of the crystal. The pyramid structure is the simplest of these structures.

Given the characteristic properties of crystal growth in the Au/polysilicon system it is interesting to imagine some practical applications. One possible use of the Au/polysilicon growth process is the fabrication of silicon on insulator (SOI) structures. It was shown in section 5.3 that crystals can be grown (conformally) over a step. Based on this and the fact that the crystals can be seeded via a selected area on the substrate, the process sequence outlined in Fig. 5.6 is suggested for the construction of SOI structures. This process would produce individual (100) Si crystals isolated from each other via an insulating (SiO_2) layer.

Another possible set of applications use the result that the crystals grow initially in the shape of pyramids. The sharpness of the tip of the pyramids is the characteristic of interest. The first application is for use as the primary tip in indenting machines. These tools are used for the analysis of the mechanical properties of material. The second use for these sharp pyramids is for field-emitting cathode tips used in micro-vacuum-electronics devices[8,9] shown in Fig. 5.7 (e.g. flat panel displays, transistors, etc.). These devices work on the principle that the tip will emit electrons when voltage is applied to the pyramid because of the high electric field at the tip.

Possible Applications

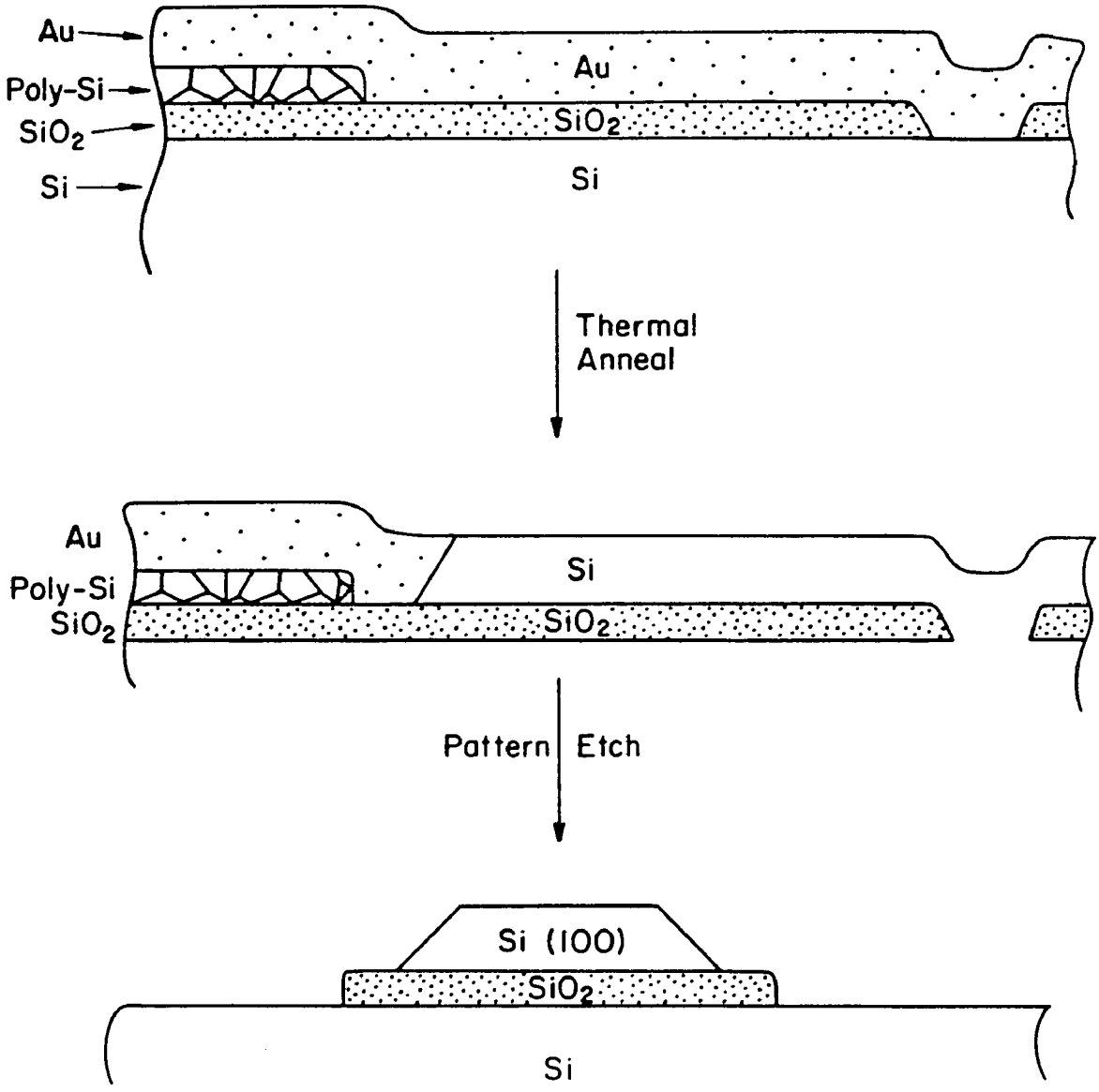
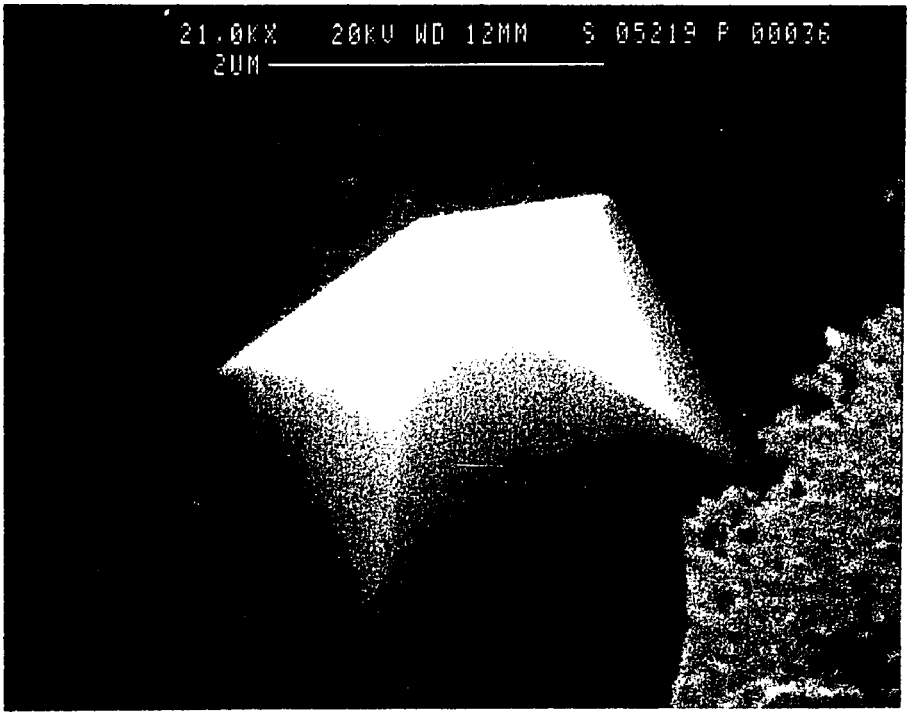


Figure 5.6 Diagram of possible process using the Au/polysilicon system to produce SOI (Si On Insulator) type structures.

(a)



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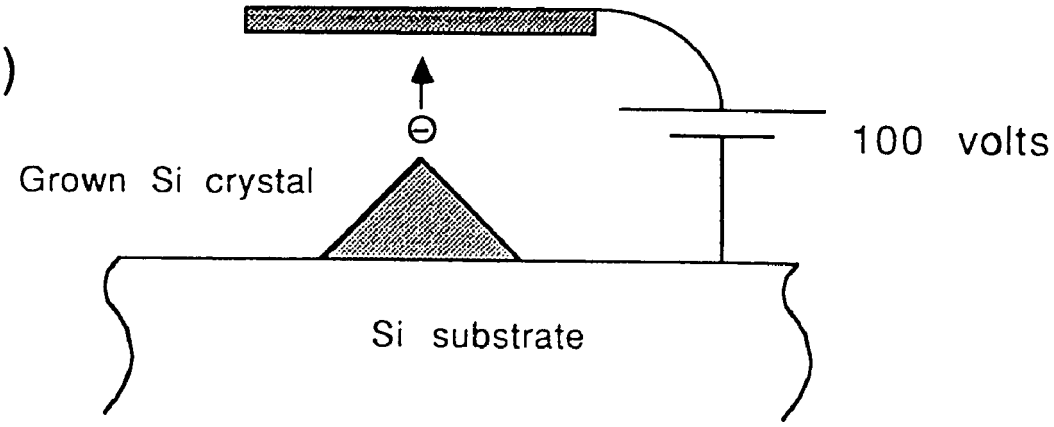

Figure 5.7 SEM micrograph (a) of Si pyramid grown from a seed area on the substrate. The crystal was grown in a thick (>1μm) layer of Au. Schematic diagram (b) of a possible application of the pyramid crystal if the tip of the pyramid is sufficiently sharp - a field-emitting cathode device.

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Chapter 6

Au redistribution during thermal anneals of Au/polysilicon bilayers

6.1 Introduction

In the analysis of Si[1,2] crystal growth process in chapters 3 and 4, little was said concerning the role of the Au layer in crystallization process. This section focuses on the characteristics of the Au layer during thermal anneals. Three topics will be explored in this chapter. The first section deals with the changes in the Au layer (grain growth) occurring at the initial stages of the anneal before Si crystallization is significant. The second section deals with the morphological rearrangement of the Au layer, changing from a relatively flat uniform layer to a complex three dimensional structure. Finally, the topic of diffusion paths of the Si through the Au layer is reviewed.

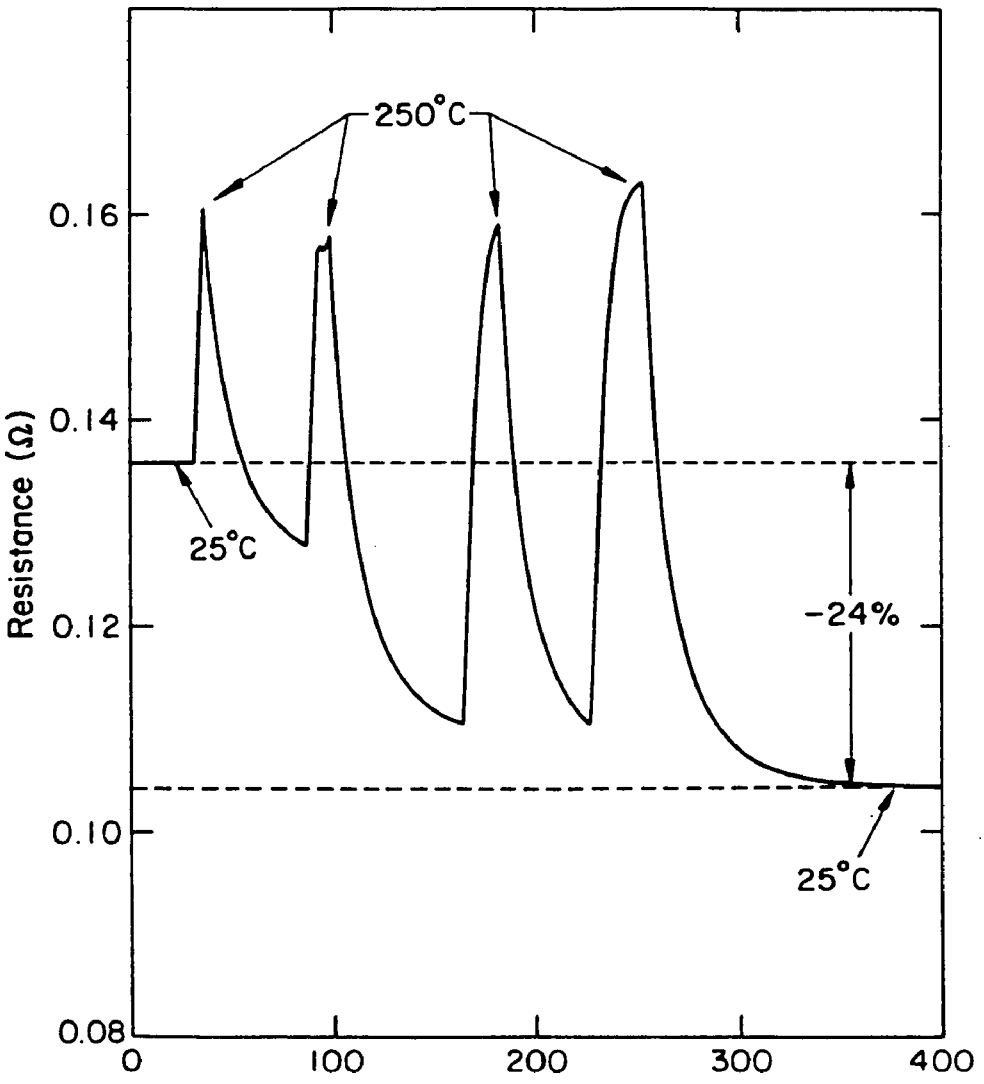
6.2 Changes in Au microstructure during initial stages of anneal

In an earlier section, it was explained that the Si crystal growth process was monitored via the change in sheet resistance. In analyzing the data, the resistance values are normalized to the value measured at the time the sample had reached the anneal temperature. As the temperature of the

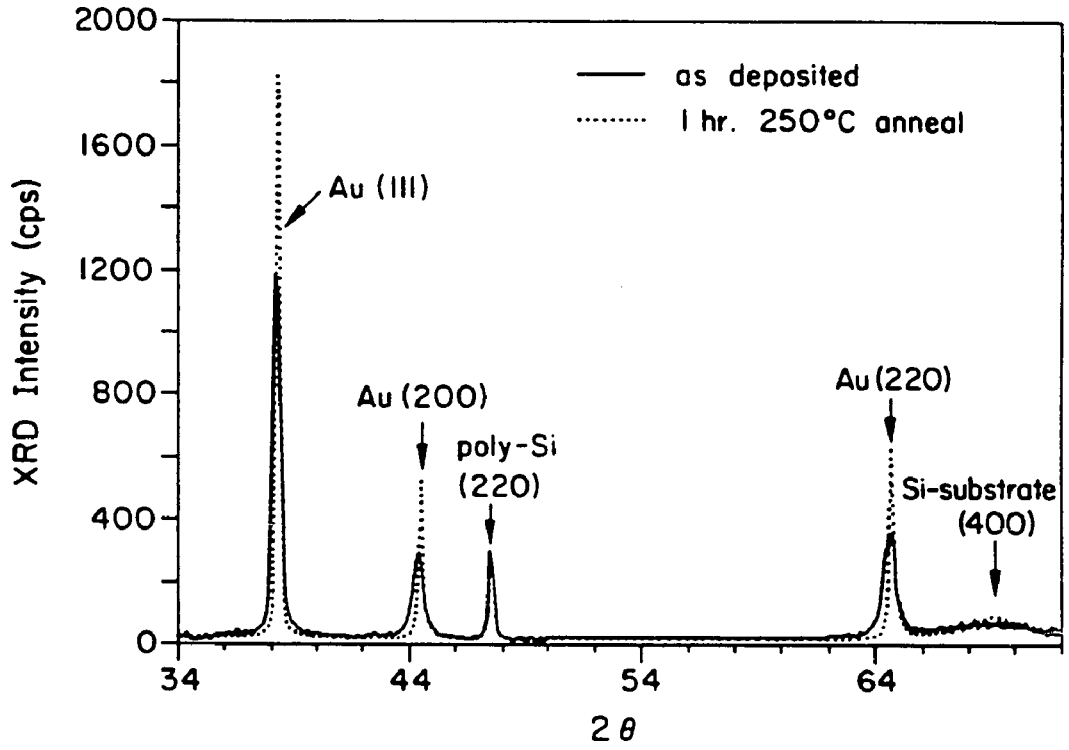
sample is increased during the heat-up period the resistance of the Au layer increases, this is expected since Au has a positive temperature resistance coefficient ($(\Delta r/\Delta T)/r \approx 0.004°C^{-1}$). But upon immediate cool down of the sample, the resistance-temperature curve did not retrace itself. The room temperature value of resistance of the annealed sample will be lower than the as deposited sample. This effect is demonstrated in Fig. 6.1, where the as-deposited sample is cycled to and fro the anneal temperature (270°C) for short periods of time. There is a 24% decrease in room temperature sheet resistance value, most of which occurs in the first stages of the heat-up. The total accumulative anneal time is less than 1 hour.

The change in resistance is not due to the change in shape of the Au layer as a consequence of Si crystal growth, since the Si growth process is only in the initial stages (≥1%) of completion. RBS and the SEM inspection of the free-standing Au films showed no significant changes in the shape of the layer. Therefore it is concluded that the decrease in resistivity is due to the internal properties of the Au film. To further investigate this effect, XRD was used (Fig. 6.2) to compare the as-deposited sample with a sample annealed for a limited time (1 hour 270°C). The annealed sample shows a marked increase in XRD peak height intensity and a decrease in peak width, both of which are indicative of grain growth of the Au. Samples annealed for additional times (up to 4 hours) did not shown any additional changes in XRD characteristics.

In order to verify that grain growth was occurring in the Au film, a TEM study was initiated. New samples (500 Å of Au on single crystal Si) were prepared and annealed at 200°C for an hour. XRD analysis of these type samples also showed an increase of peak height intensity after thermal annealing. The data showed that the films had a strong (111) preferred



Figures 6.1 In-situ 4-point probe resistance of Au film (Au/polysilicon/SiO_2) during thermal cycling (25°C-250°C) experiment. The temperature coefficient of resistance is a factor in determining the value of resistance but the net decrease of resistance (-24%) is due to the increase in size of the Au grains.



Figures 6.2 XRD diffraction of (Au/polysilicon/SiO_2) samples as deposited and samples with 1 hr. 250°C anneal. There is an increase of peak intensity and decrease in peak width for the Au peaks indicative of grain growth. The shape of the (220) Si peak from the polysilicon does not change since there is minimal interaction between the Au and polysilicon at this early stage of the anneal.

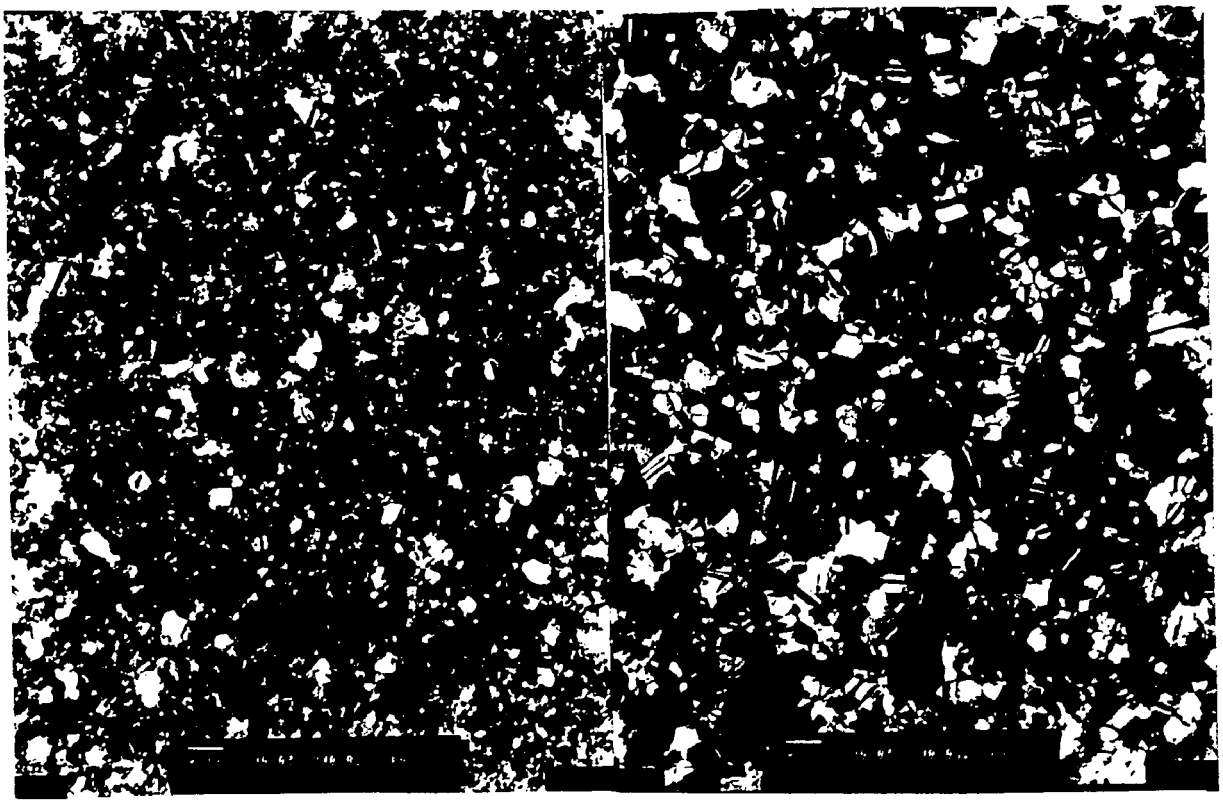
orientation for both the as-deposited and annealed samples. TEM plane view micrographs, shown in Fig 6.3, show significant grain growth as the result of the anneal. A plot of the frequency vs. grain diameter is also shown in the figure. Low temperature grain growth has been investigated for Au thin films deposited on SiO_2 substrates by other investigators[3] where substantial grain growth was observed in the Au even at 25°C.

The 24% increase in the conductivity of the annealed samples is speculated to be due to the increased effective average mobility of the carriers due to the increase in the average grain size of the Au.

6.3 The redistribution of Au during thermal anneal

Substantial changes in the shape of the Au layer occurs after extended thermal annealing, when Si crystal growth occurs. There is a one to one exchange between Au and polysilicon, no hillocks or voids are observed. The initial exchange between Si the Au is not symmetric. Si displaces the Au from the original Au layer in the form of two dimensional crystals, whereas the Au displaces the Si in the form of vertical spikes.

If the reaction between the layers proceeded via a layer by layer process the analysis would be straightforward, but because the redistribution of the Au is laterally and vertically nonuniform, analysis using the typical methods (RBS, AES, etc.) proved to be difficult. For example, RBS spectra of a series of Au/polysilicon/SiO_2/Si samples annealed for different times are shown in Fig. 6.4-a. The Au peak for the as deposited sample is well defined, but as the reaction proceeds a broad tail develops at the trailing edge of the peak. Deconvolution of the RBS data by itself is



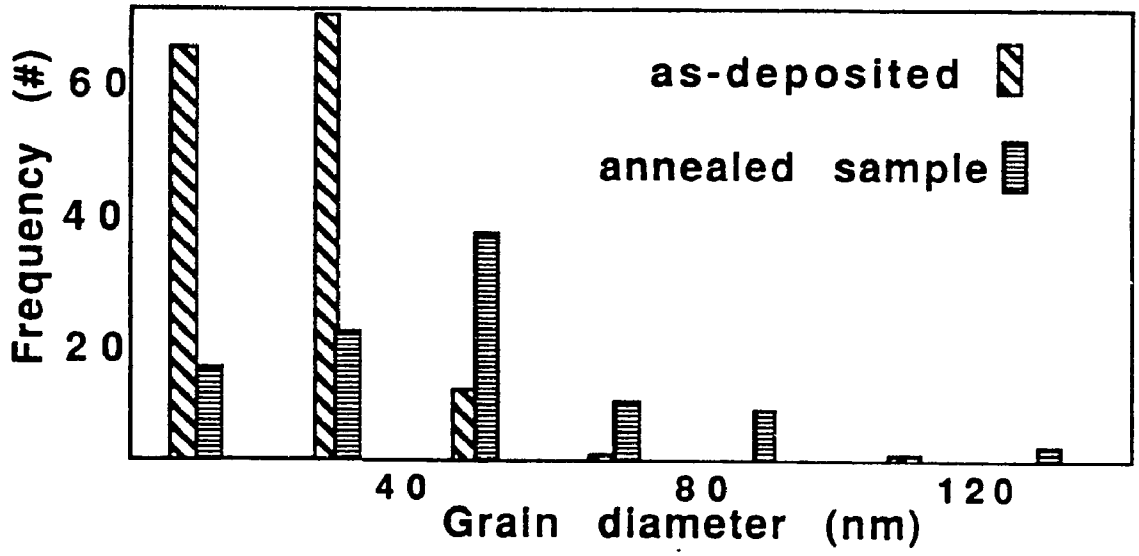


Figure 6.3 Planar TEM micrographs of as-deposited and annealed (250°C for 60 min.) samples. The histogram details the frequency vs. grain size of the films and shows that there is substantial increase in grain size as a result of the anneal.

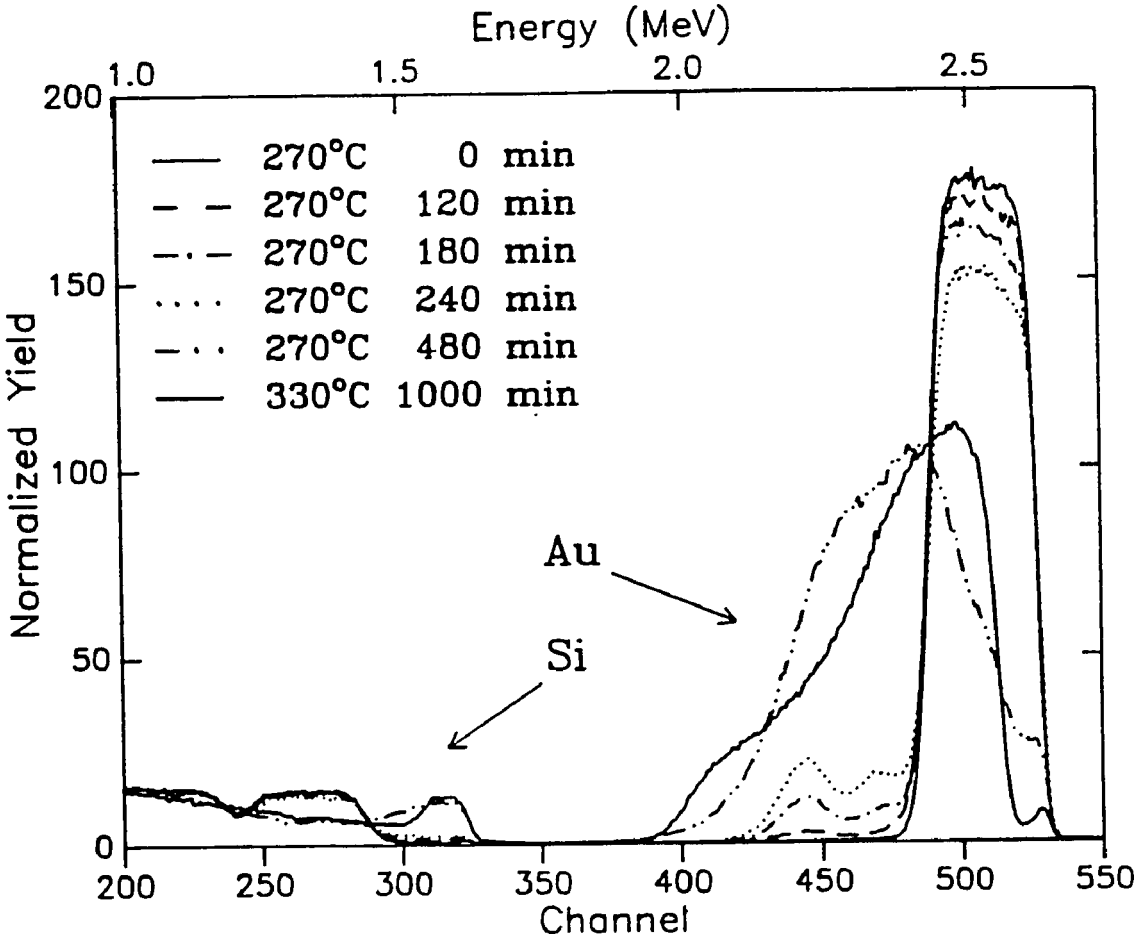


Figure 6.4 RBS spectra of Au/polysilicon samples annealed at different times and temperatures.

almost impossible as it yields a variety of possible different interpretations, so other methods of analysis are used in parallel with the RBS technique.

The most useful and direct method of determining the shape of the reacted Au film is via SEM analysis of free standing Au films. This technique involves the separation of the entire Au film from the polysilicon layer and the substrate. This is accomplished by submerging the entire sample into a solution of HF (48%) and HNO_3 (1%) acids. The polysilicon, SiO_2 and Si dissolves easily in this solution releasing the entire Au film intact, which is then retrieved from the solution using a standard TEM sample grid. A three dimensional model of the shape of the film can then be reconstructed from SEM micrographs taken of sample from different angles. For example, in Fig. 6.5 pictures of both the top (a) and the bottom [(b) and (c)] of the Au layer were obtained from the same sample by simply flipping the TEM grid (which supports the free standing Au film) during the SEM examination.

By analyzing the RBS and SEM data, a three dimensional model of the physical shape of the Au can be reconstructed. Shown in Fig.6.6 is a cross-sectional, time-sequence model of the Au layer as the reaction progresses. Note that the Au initially penetrates into the poly Si layer via sharp (1000Å diameter) vertical spikes. Then as the spikes extend to the bottom of the polysilicon layer, at the polysilicon/SiO_2 interface, the Au spreads along the bottom of the polysilicon. A SEM picture which simultaneously shows the top and bottom view of a partially annealed sample is displayed in Fig. 6.7 (a). (This particular sample folded onto itself as the sample was retrieved from the acid solution.) Note that Au forms an almost continuous layer at the bottom, polysilicon/SiO2 interface. The observation of Au at this interface is confirmed by RBS spectrum shown in Fig. 6.8. This Au interface layer has a

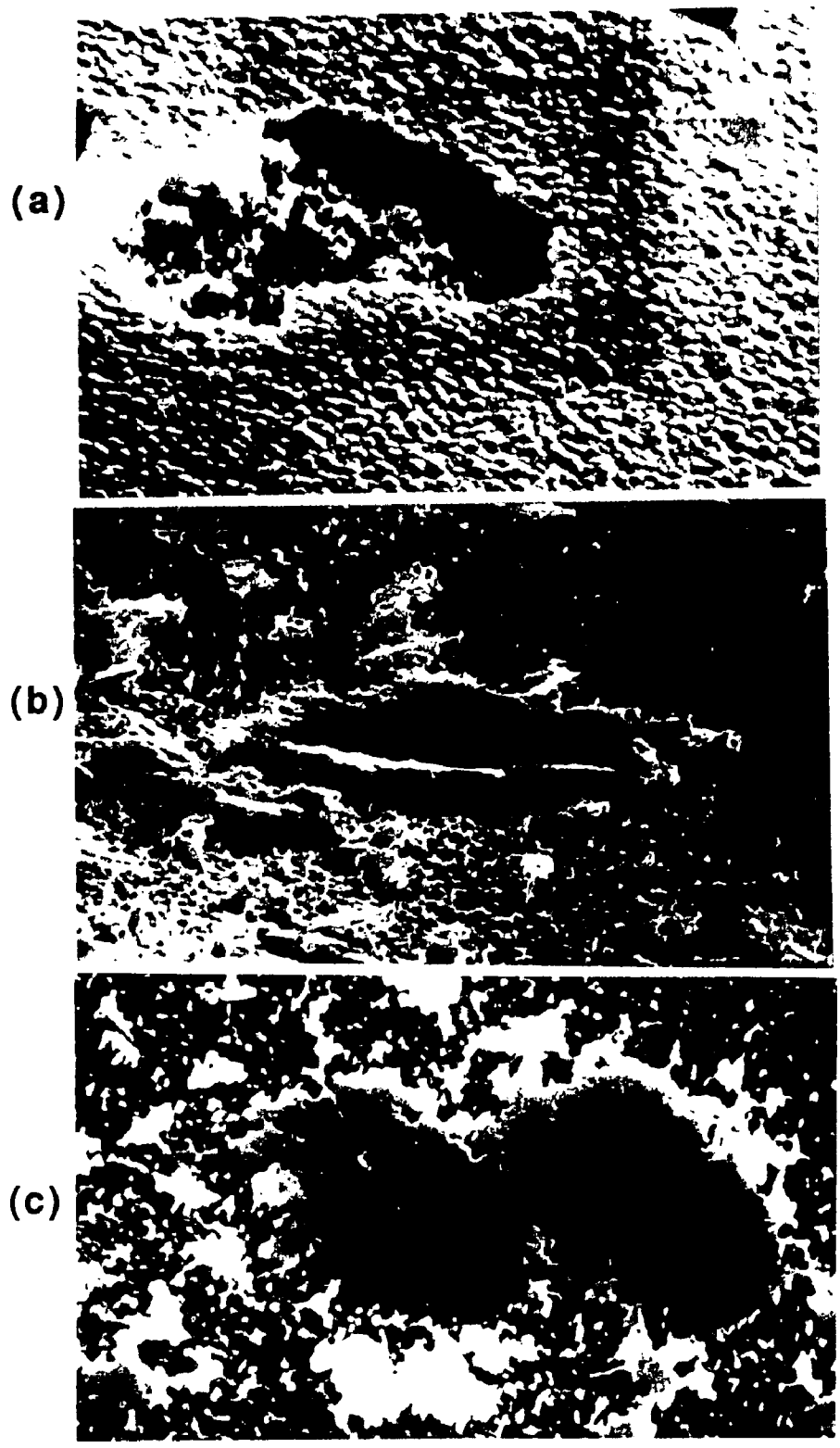


Figure 6.5 SEM micrographs with view from the top (a) and bottom [(b) and (c)] of partially annealed samples. These free-standing Au films were obtained removing the Au film from the Au/polysilicon/SiO_2 structure by etching the samples in an acidic solution of HF and HNO_3.

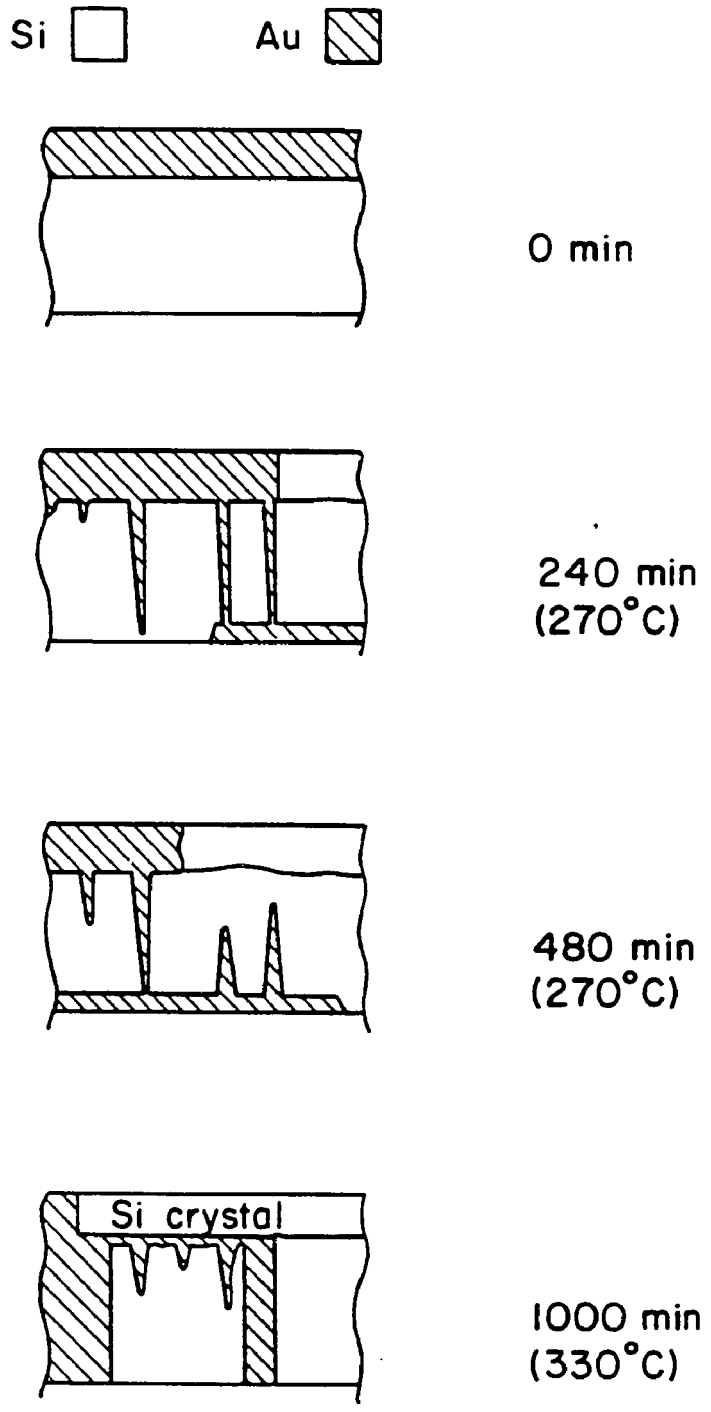


Figure 6.6 Model of the sequence of redistribution of the Au and Si during thermal annealing.

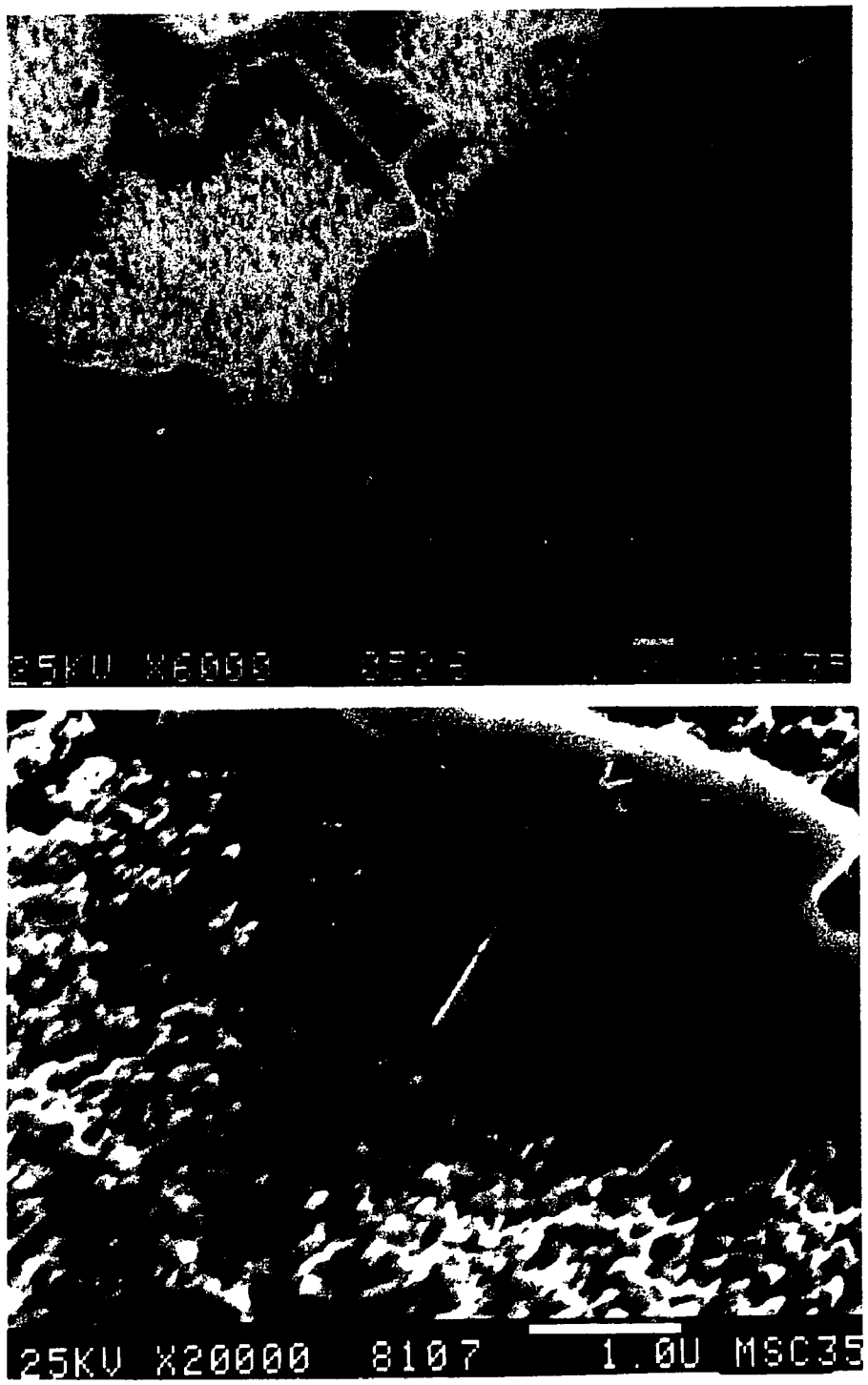


Figure 6.7 SEM micrographs of free standing Au films. of partially annealed sample (a) of both top and bottom view of a film folded on to itself showing the spikes of Au penetrating the polysilicon region.. Also shown (b) is the bottom view of a fully annealed sample, note the smooth surface of the mass of Au, smooth because it was located at smooth Si interface.

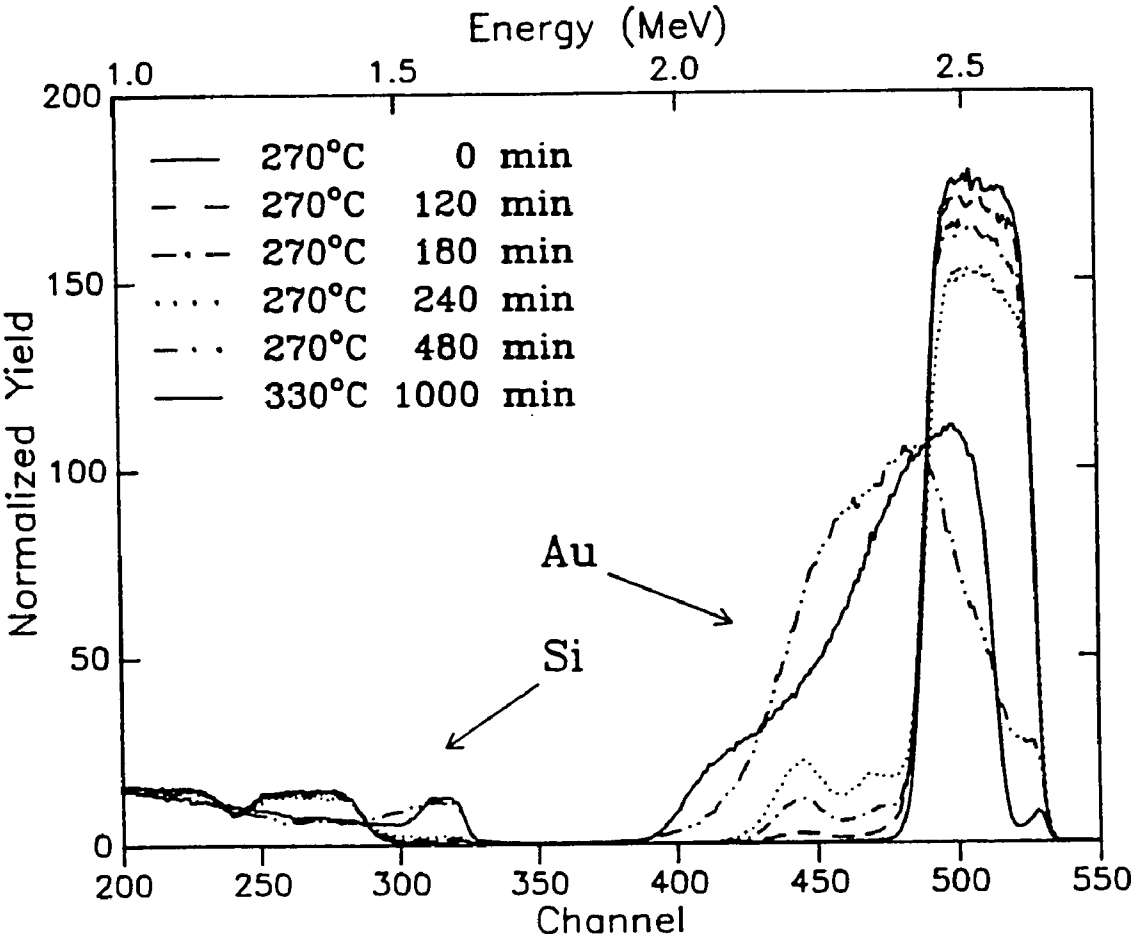


Figure 6.8 RBS spectra of partially and fully annealed samples with inset diagram identifying the location in the structure with position of RBS signal. Note that the Au diffused through the polysilicon (via spikes) to form a thin Au layer at the original polysilicon/SiO_2 interface.

thickness of a few thousand Å and is smooth on the SiO_2 side as shown in Fig.6.7 (a) and (b).

Given that the sequence of Au redistribution is known, what can we deduce from this data regarding the basic parameters of the reaction (i.e. driving forces, diffusion paths, etc.). For example, why does the Au form a layer at the polysilicon/ SiO_2 interface. One idea suggests that the chemical potential of the Si at the polysilicon/ SiO_2 layer is high due to interfacial energy between the polysilicon and SiO_2. In fact it has been speculated that this interfacial energy is responsible for the main driving force of the entire reaction, that the Au/SiO_2 is lower than the polysilicon/SiO_2 interfacial energy. Inspection of samples in the final state, after extended annealing [Fig. 6.7 (b)], shows that the Au at the polysilicon/ SiO_2 continues to redistribute (upon continued annealing) into isolated Au islands. Therefore it is concluded that the interfacial energy is not the key parameter (driving force).

It is believed that the Si at the initial polysilicon/ SiO_2 is different than the Si in the remaining polysilicon layer in terms of the degree of crystalline order. CVD Si is essentially a nucleation and growth process where the initial Si layers consists of small grains. Continued deposition results in fewer but larger grains tending toward a columnar structure. Texturing occurs[4] as the film thickness increases and for films grown at 620°C the grains develop a [110] preferred orientation. It is deduced from this that there are, on the average, more defects (grains boundaries) in the initial layers of the ploy-Si film than on the subsequent layers. Because of this the chemical potential of the Si is higher in the region of the interface because it consists of the initial layers of the deposition. The average chemical potential of the Si decreases as the film thickness increases in a continuous way as the gain size increases.

6.4 Diffusion paths of Si through Au layer

Si crystallization is a result of long range lateral transport of Si through the Au layer. This description of the Si diffusion process is stated in general terms because the mechanism of atomic transport is not known. The possibilities include bulk diffusion through the grains and diffusion via the grain boundaries. Surface diffusion may also play a role but the top surface of the Au is probably not a free surface since SiO_2 is most likely covering the entire Au surface. A small Si surface peak has been observed routinely on as deposited Au/polysilicon samples, in fact this SiO2 layer is easily observed qualitatively by visual inspection when the samples are left exposed to ambient air at room temperature for a few months.

A different diffusion path which is schematically pictured in Fig. 6.9 is one which is related to the Au/Si interface. This type of two dimensional diffusion path is considered important because of the unusual nature of system. Au melts at 1337°K and Si melts at 1683°K but together they melt at approximately 640°K (eutectic temperature). The large difference in the melting temperature between the components and the combination of components is a curious characteristic of deep eutectic systems but perhaps even more interesting in the case of the Au and Si system because of the extremely low solubility of each component in each other.

The Au/Si interface has been studied using AES and XPS on thin layers (<500Å) of Au on single crystal Si. It has been concluded[5,6] that the interface is not abrupt but is a diffuse region having a width of approximately 50-100 Å. The Si atoms in this region form metallic bonds with the Au, similar to the case of Si in metastable Au-Si compounds. This diffuse region at the Au/Si interface is not unique, it is also observed[7] in the Al/Si

system which also forms a eutectic system.

To estimate the feasibility of this layer as a conduit for the Si flux measured in the earlier chapter we estimate the diffusion constant D. The flux rate of the growing crystal is of the order 1Å/sec. If we assume for the sake of argument that the width of this region is 100Å and concentration gradient is 10^{22} atoms/1μm then the diffusion coefficient D is calculated to be of the order 10^{-11} cm^2/sec, which is a reasonable value.

6.5 Conclusions

Changes occur in Au films during thermal annealing of Au/polysilicon bilayers. The first measurable change occurs within the Au layer and is probably not directly related to the bilayer structure. In the initial stages of the anneal before the Au and Si interact, the grain size of the Au increases. This is observed in three ways: an increase in the grain size (TEM), a decrease of resistance, and a sharpening of the diffraction peaks (XRD).

After extended anneal times, the bilayer components Au and Si begin to interact resulting in the second major change in the reaction. Si recrystallization occurs with the subsequent redistribution of the components. The Au interchanges with the polysilicon using a one-to-one displace mechanism which conserves the morphology of the composite layer. Spikes of Au protrude the polysilicon layer as the Si dissolves and recrystallizes.

The path of the diffusion is not known but is expected to be due to a combination of bulk, grain boundary, and interface processes.

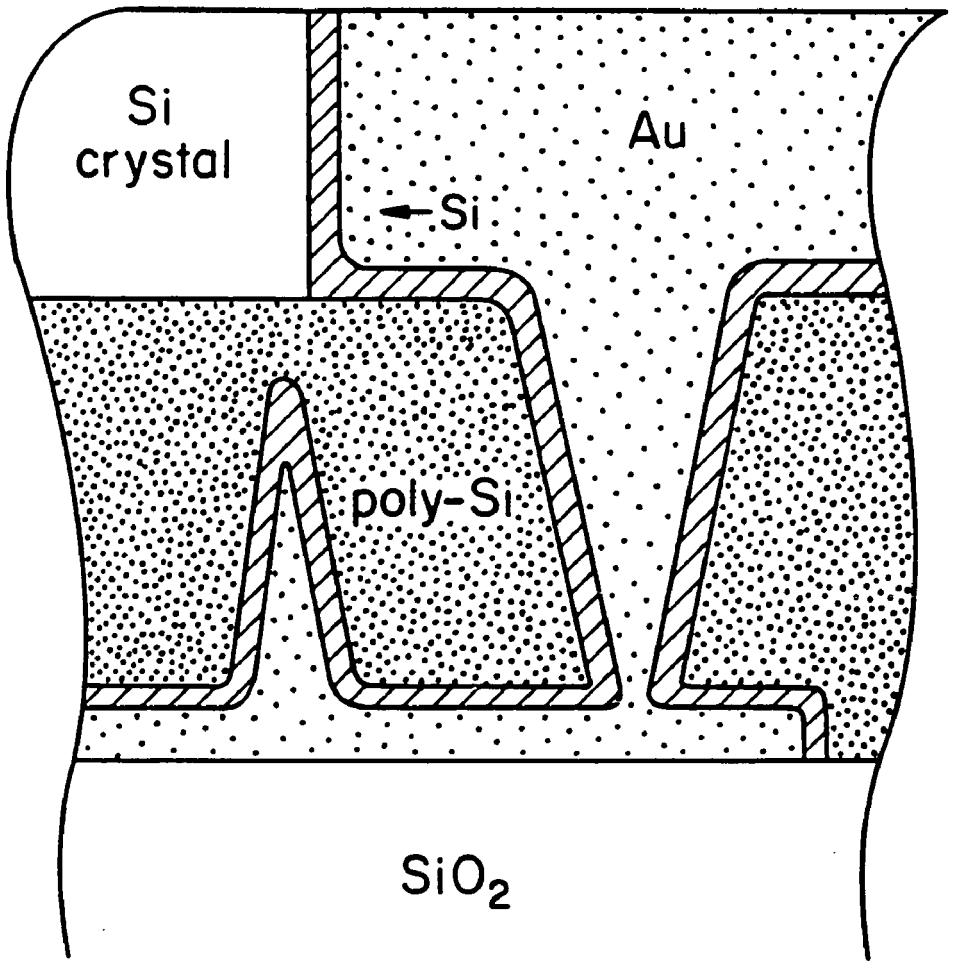


Figure 6.9 Model of interface diffusion path of Si through the Au layer. This model proposes that Si diffusion may occur via a thin (50-100 Å) interface layer which is shown in the diagram by the region in cross-hatched marks.

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Part II

Interface contact resistance studies

Chapter 7

Introduction

7.1 Introduction

The importance of interfaces and surfaces has paramount importance in many applications. Surfaces are of importance because many of the interfaces of interest are created by depositing thin films of material onto the surface. This initial surface, which later becomes an interface, is almost always of primary importance. The region at an interface may be extremely thin, consisting of only a few layer(s) of atoms, but may dominate the outcome of the entire reaction kinetics, adhesion and/or the electrical characteristics.

Interest in interfaces for this paper falls into two general areas : surface contamination prior to CVD W deposition (chapter 10), and ohmic contact formation at the metal/ *n*-GaAs interface (chapter 11). In both cases the thin region at the interface controls the characteristics of the device/reaction.

Direct methods for analyzing the interface include RBS, AES and SIMS. An indirect method, which also can be used to probe the interface, is the measurement of contact resistance. This method can be extremely sensitive to thin layers (e.g. insulating) or small changes at the interfaces, it has the advantage of having a broad measurement range (10^6). It's major disadvantage is that it is an indirect method, and usually requires models

and/or critical assumptions in order to interpret the data.

Typical methods of measurement of contact resistance will be reviewed in the chapter 8. A new method of contact resistance measurement, which in some cases has definite advantages over the other methods, will be introduced in chapter 8.

One problem with any contact resistance measurement is concerns the assumption of current uniformity. This problem is addressed and analytically solved (chapter 9) for a particular type measurement structure - those with radial current symmetry (circular vias).

These contact resistance methods are used to evaluate the interface (chapter 10). Here we seek to evaluate the problems related to the selective CVD growth of W on Al surfaces. The study combines the electrical information with SEM and preliminary AES results.

The final chapter in the thesis presents some of the work done with GaAs. Here again, the interface is of primary importance. Relatively good contact resistance values ($\rho_c \approx 10^{-7}\ \Omega\ cm^2$), were obtained early on in the study. The material analysis of the reaction required more time and has not been published yet. Most of the difficulty in the analysis was due to the nonuniform morphology of the top metal (indium and palladium) surface, which disabled most analysis tools (RBS, AES,etc.). Indium, as deposited (25°C), grows in large crystals producing a very rough surface. Smooth surfaces were eventually obtained by evaporating the indium at liquid nitrogen temperatures, and these samples were useful for channeling experiments. Two other techniques were also very useful; XRD and backside SIM profiles.

As was the case for Part 1, each chapter includes an introduction section, which addresses each set of problems in more detail.

Chapter 8

New thin film contact resistance measurement

8.1 Introduction

Several methods[1] are currently being used to measure contact resistance of metal/metal and metal/semiconductor interfaces including Kelvin method[2] and the Stack and Cox method[3]. Recently another method[4] similar to Stack and Cox was proposed and used to measure the contact resistance between thin film metal and a bulk semiconductor. Based on this idea, we developed a new method[6] which can be applied to thin film/thin film contacts. In order to verify the accuracy of the new method, referred to here as the spreading resistance "SR" method, a comparison is made with the standard four terminal Kelvin structure. The comparison is made on two layer Al/Al contacts.

The new SR method serves to compliment the standard Kelvin method. In some cases the new method circumvents some of the fabrication and analysis problems associated with the Kelvin method, while in other cases the new method is expected to be less sensitive to low contact resistances. The Kelvin method essentially requires two independent pairs of narrow lines to be connected to the top and bottom of the via. Because these lines need to be carefully aligned to each other, there is a need for strict tolerances in both the photolithographic process and the level to level registration specifications of the photomasks. Furthermore the analysis of

the data from the Kelvin structures is in some cases difficult[2] (e.g., current crowding) because of the lack of symmetry in the basic design of the structure. A complete analysis of current crowding in Kelvin structures would require 3-dimensional numerical analysis techniques which are very difficult.

The structures needed for the SR method do not require strict tolerances and therefore are easier to fabricate. In contrast to the Kelvin structures, the SR structures are designed to have cylindrical symmetry which simplifies data analysis in the case of current crowding.

In this chapter the Kelvin and the SR method described and compared noting the advantages/disadvantages of each method. The problem of current crowding in circular vias is analyzed in the following chapter and we obtain analytical solutions which predict the correct value for the contact resistivity parameter P_c.

8.2 Experimental

The devices discussed in this study were fabricated by a three level process. The bottom layer pattern was produced using the lift-off technique, 3,000 Å of Al was sputter deposited onto a thermally oxidized Si wafer which was patterned with photoresist. A blanket layer of SiO_2 (0.5 μm) was then sputter deposited onto the sample and patterned by etching with a RIE process to form the circular contact vias having radii of 1.0, 1.2 and 1.3 mm (+/- 0.1 mm). For the top metallization the sample was first sputter cleaned and then Al was again sputter deposited using a lift-off technique. The resultant layered structure consisted of two layers of Al separated by an

insulating SiO_2 layer, the two metal layers being directly connected to each other by a small via through the insulating layer. The Al/Al contact was chosen for this study in order to obtain the smallest possible values for the interface resistivity P_c which should be low in this case. Low resistance contacts were needed to evaluate the sensitivity of the new method.

In order to increase the accuracy of alignment between levels, the photomasks were fabricated with electron-beam technology with level to level registration of +/- 0.2 mm. Sheet resistance measurements of both top and bottom Al layers are critical for the SR method. Four equally spaced vias, arranged in-line were used to determine the bottom Al layer sheet resistance in an analogous way the standard 4-point in-line probe measurement is made. In order to measure the sheet resistance of the top metal layer a serpentine structure was used.

8.3 Kelvin Resistance Structure

A common problem in any type contact resistance measurement is the separation of the contact resistance R_c of the via, which is of most interest, from parasitic resistances. These parasitic resistances are extrinsic to the via and are due mainly to the voltage drops along the current path which connect the vias to the probe pads. Kelvin structures (Fig. 8.1) are designed so that only the contact resistance of the via is measured. In the ideal structure, the sense (voltage V_s) leads measure only the vertical voltage difference across the via. The contact resistance R_c is then directly evaluated using Eq. (8.1).

$$R_c = V_s/I \tag{8.1}$$

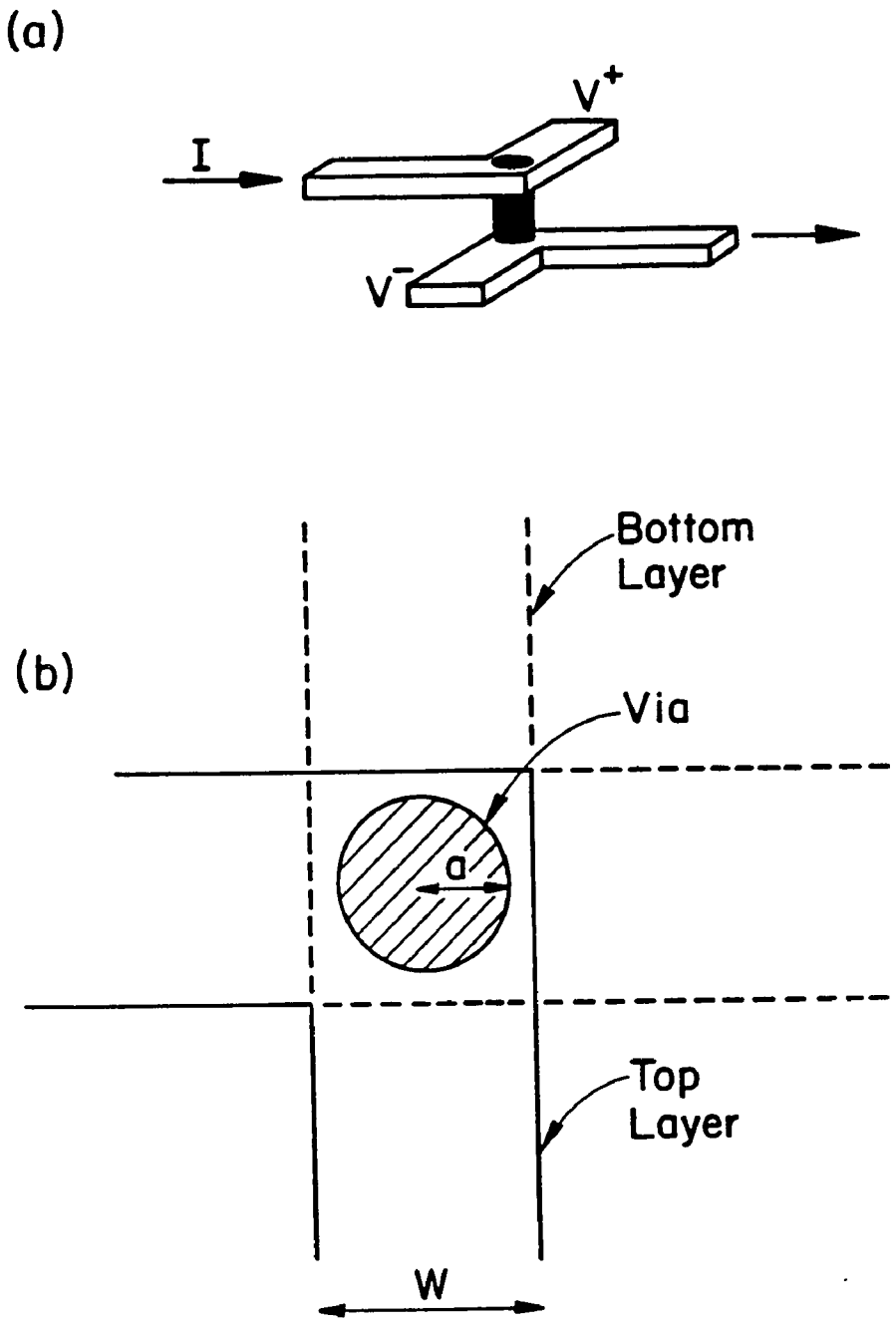

Figure 8.1 Kelvin resistance structures used in this study, (a) side view and (b) top view. The width of the lines is "w" and the radius of the via is "a".

where I is the total current to the via.

To obtain accurate values for low contact resistances small via diameters (1-10 mm) are required. Furthermore, in the case of the Kelvin structure, it has been shown [2] that for improved accuracy the sense and drive lines must be of the same size as compared to the via. It is also necessary that the via level be accurately centered with the top and bottom metallization lines. To satisfy these requirements it is essential to precisely align the levels to one another. It is especially important in certain types of metallization processes such as the CVD selected tungsten deposition where misalignment may cause unexpected growth characteristics of the via (plug) metal. In practice, to insure complete overlap between via and lines, the width of the lines are made slightly larger than the via. This is done at the expense of the accuracy of the measurement. Two types of Kelvin structures KA and KB were fabricated for this study, line widths (w) exceeded the via diameter (2a) so that (w-2a) was 1 mm (KA) and 2 mm (KB). All critical dimensions used in this paper where measured using an SEM.

8.4 Spreading Resistance Structure

The new contact resistance method SR provides, in some cases, an alternative to the Kelvin method. Choosing which method to use will depend on the system that is being tested. The Kelvin method should always be applicable but the structures will be more difficult to process and the data will be more difficult to analyze in the case of current crowding.

In contrast to the Kelvin structures where the current is confined to a narrow path to and from the via, the current path in the SR structure is open.

The combined via and parasitic resistance are measured together. Because of the design and symmetry of the SR structure the parasitic resistance can be accurately determined and then subtracted from the total resistance yielding the via resistance.

Many different types of SR structures could be used to measure R_c. The structure used in this study (Fig. 8.2a) consists of a chain of vias connected in series. Also shown in Fig. 8.2b is the equivalent resistance network containing the contact resistance R_c and the parasitic resistances R_{spo} and R_{sp2} which are due to the spreading resistance near the vias at the top and bottom metallizations. The total resistance for each unit of the chain can be expressed as

$$R_T = 2R_c + R_{spo} + R_{sp2} \tag{8.2}$$

After the total resistance R_T and the sheet resistances R_{sho} (bottom) and R_{sh2} (top) of the Al layers are measured, the spreading resistance factors can be calculated and subtracted. The key feature which makes SR method easy to apply is that the spreading resistance is well defined by the geometry of the structure and can be easily evaluated. The spreading resistances R_{sp} for two vias of radius "a", separated by a distance "s" situated on a planar thin film (Fig. 8.2c) is given by

$$R_{sp} = K R_{sh} \ln(s/a) / \pi \ , \tag{8.3}$$

where K is a correction factor determined by the geometry of the lamina. If the vias are situated on a pad which is much larger than the spacing "s" then $K = 1$. In our particular structure the vias are placed within a square $(98\ mm)^2$ pad and have a spacing of 50 mm. Using 2-dimensional numerical techniques, the correction factor was found to have a value of K=1.07. By using Eqs. (8.2) and (8.3) the contact resistance R_C can be obtained.

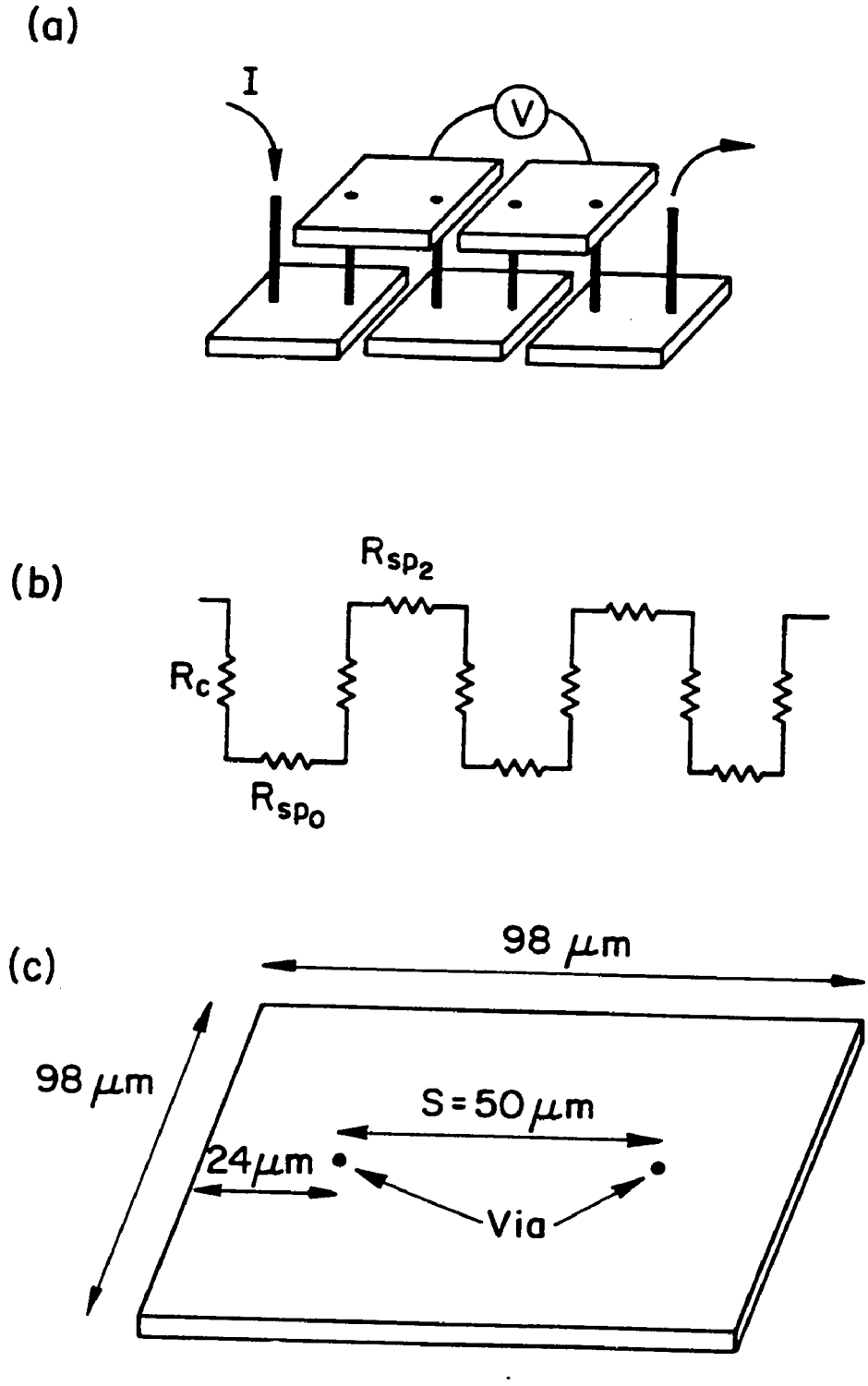

Figure 8.2 The resistance chain (a) used in the SR method with the equivalent resistor network (b). The dimensions (c) of a segment of the chain are also shown.

8.5 Results

A demonstration in the use of the SR method is shown in Fig. 8.3. Using the chain structure (Fig. 8.2a), current was applied to endpoints of the chain, the voltage difference was sensed for each individual chain segment. Values for the total resistance $R_T = V/I$ for the individual segment were consistent across the chain, varying less then 2% over the entire chain.

Spreading resistance values were evaluated using Eq (8.3) with the values for sheet resistance obtained from structures adjacent to the via chains. By subtracting the spreading resistance from the total resistance we obtain the values for the contact resistance per via as a function of via size (Fig. 8.3). The solid line in Fig. 8.3 is a plot of R_c vs via radius given that $R_c = P_c/(\pi r^2)$ and $P_c = 0.07\ \Omega\text{-mm}^2$.

We also note the disadvantages of the SR method by observing that a large fraction of the total resistance is due to the spreading resistance factor. Since both the resistance parameters R_T & R_{sp} have a measurement error associated with them, if the two have comparable values the difference R_c may be extremely small, accompanied by a large error, and therefore highly uncertain. In effect, the sensitivity of the measurement of R_c is limited by the value of spreading resistance, for example the minimum detectable value for R_c would be some fraction (e.g., 5%) of R_{sp}.

When the SR measurements are compared with the Kelvin structure measurements in Fig. 8.4 and Table I, good agreement is observed. The error bars in Fig. 8.4, represent the standard deviation of measurements taken at different locations on the wafer. From the data it can be seen that the variation in the measured contact resistance for a given via radius is larger for the Kelvin measurement and decreases as the via increases.

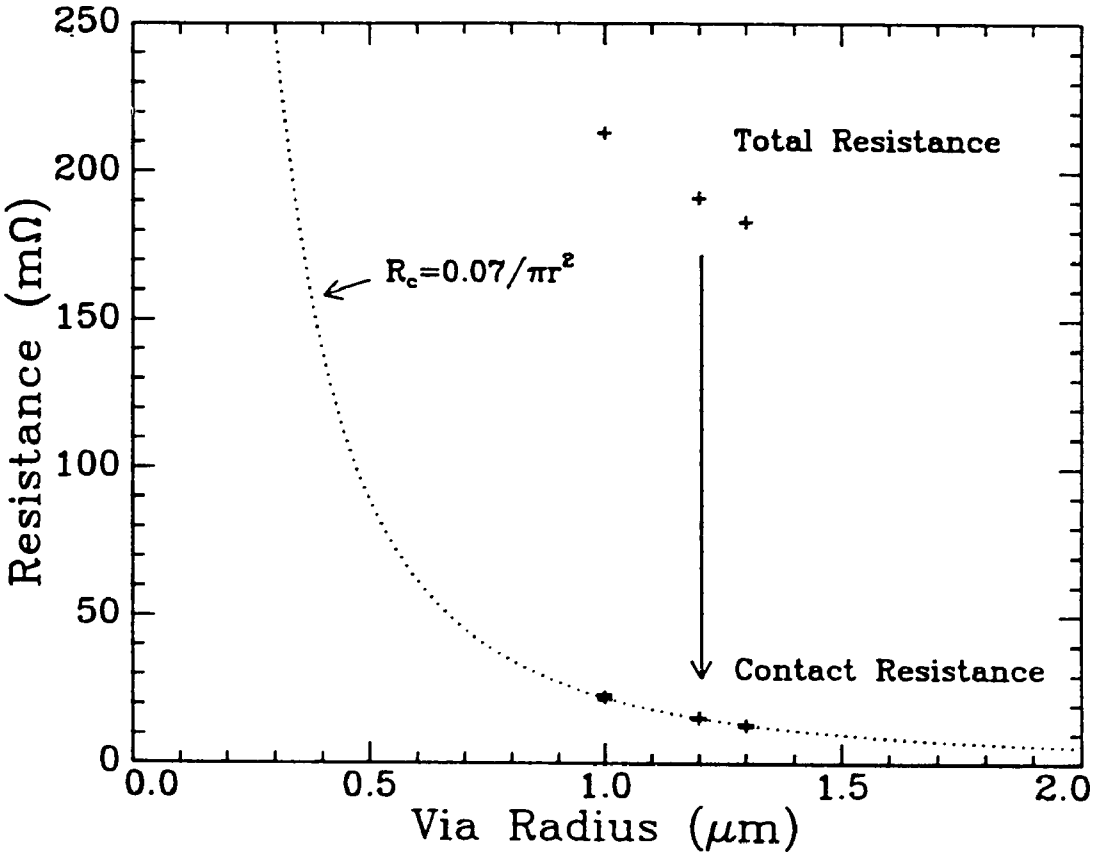

Figure 8.3 Experimental data of the total resistance and contact resistance vs. the radius of the via. The solid line is a plot of $R_c=P_c/(\pi a^2)$ where P_c $=0.07\ \Omega\text{-}\mu m^2$.

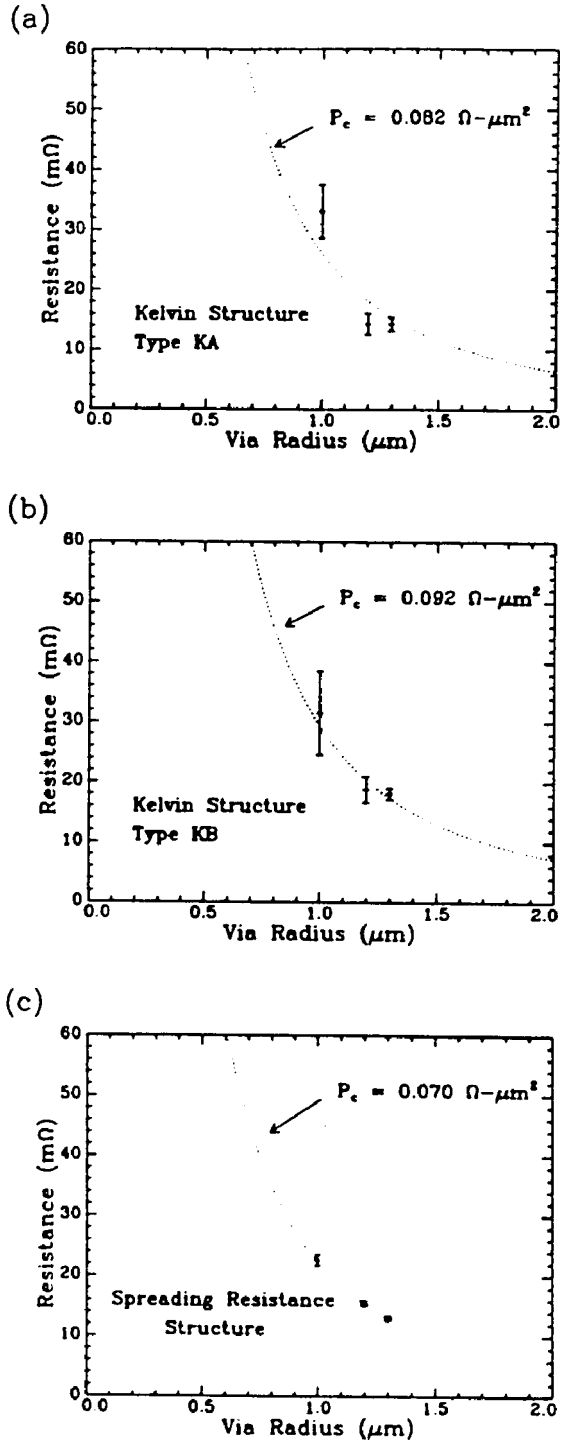

Figure 8.4 Contact resistance using the Kelvin structures type KA (a) and KB (b), and the spreading resistance (c) structure. Note the wide variation in the data for the Kelvin structures which is due in part to misalignment of the levels.

Table 8.1 Comparison of the average contact resistivity P_c calculated from the contact resistance R_c ($P_c = R_c/(\pi a^2)$), from the Kelvin (KA & KB) and SR structures of two wafers processed separately.

	Kelvin (KA) (milli-Ω-μm^2)	Kelvin (KB) (milli-Ω-μm^2)	Spreading Resistance (milli-Ω-μm^2)
Sample 1-3	118 +/- 10	138 +/- 14	114 +/- 1
Sample 1-1	82 +/- 9	92 +/- 12	70 +/- 2

This effect is possibly due to misalignment between the top and bottom layers which is critical for the Kelvin structure. Samples 1-3 and 1-1 had misalignments of 0.3 mm and 0.6 mm respectively, these were determined by measuring (SEM) the displacements of the a vernier alignment marks.

8.6 Discussion and Conclusions

The SR method for the measuring contact resistance (< 0.1 Ω-μm^2) was presented and compares well with standard Kelvin measurement. In comparing the two methods, the SR method has the advantage of relaxing the photolithographic alignment constraints required in fabrication of the structures: the levels may be misaligned by several microns yet the measurement would yield approximately the same results. Unfortunately because it uses a subtraction technique the SR method is limited in

sensitivity to higher values of contact resistance, the limits being determined by the sheet resistance of the system. Another advantage of the SR method is the ease of analysis of the data when current crowding conditions are present.

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Chapter 9

The solution to current crowding in circular vias.

9.1 Introduction

The contact resistance R_c for a particular contact via is by itself useful, but in many cases the parameter of greater interest is the contact resistivity P_C, the area independent parameter used for scaling purposes. In general the contact resistance contains many components including the interface resistance and the effects of resistance of the metallizations within the via. Our main interest is to obtain a value for the interface resistance P_C. It is assumed for our discussion that in all cases the interface and metallization characteristics are spatially uniform.

It would seem obvious that the connection between contact resistance and contact resistivity is trivial, since we could obtain the value for P_C by multiplying the measured contact resistance R_c.by the area of the via. However this may not be the case due to the nonuniformity of current within the via.

Two dimension modelling of Kelvin structures[1] shows that there is a large error, due to current crowding, in the value for P_C using the above relation. A complete analysis of current crowding in Kelvin structures would require 3-dimensional numerical analysis techniques which are very difficult.

Current crowding analysis is much easier for structures which have circular vias, designed so as to have the current radially symmetric with

respect to the via. The spreading resistance (SR) structures[2] discussed in the preceding chapter are designed with (approximate) radial current distribution, which simplifies the data analysis for the correction for current crowding. The goal of this chapter is to obtain analytical solutions which predict the correct value for the contact resistivity parameter P_c. In order to verify the accuracy of the analytic solution, a comparison is made with computer based solutions, using 2-dimensional numerical techniques.

9.2. The current crowding problem

Assuming the thin film approximation, which will be discussed in the following section, and given that the current density is uniform throughout the via (Fig. 9.1a), the contact resistivity can be expressed as follows.

$$P_c = R_c \, \text{Area} \tag{9.1}$$

However, if the via is sufficiently large the current will not be uniform, but will be concentrated near the edges of the via as shown in Fig. 9.2a. This effect of current crowding is a consequence of the current seeking the least resistive path through the structure and the values for P_c obtained using Eq. (9.1) will be incorrect. For example in a case where there is current crowding, given the measured resistance is $R_c \approx 6$ (mΩ) and via radius is 10 μm , we would calculate $P_c \approx 1.9$ (Ω-μm^2) using Eq. (9.1). This value is $\approx$ 90% too high if the sheet resistance of the film is $R_{sh} \approx 0.1$ (Ω).

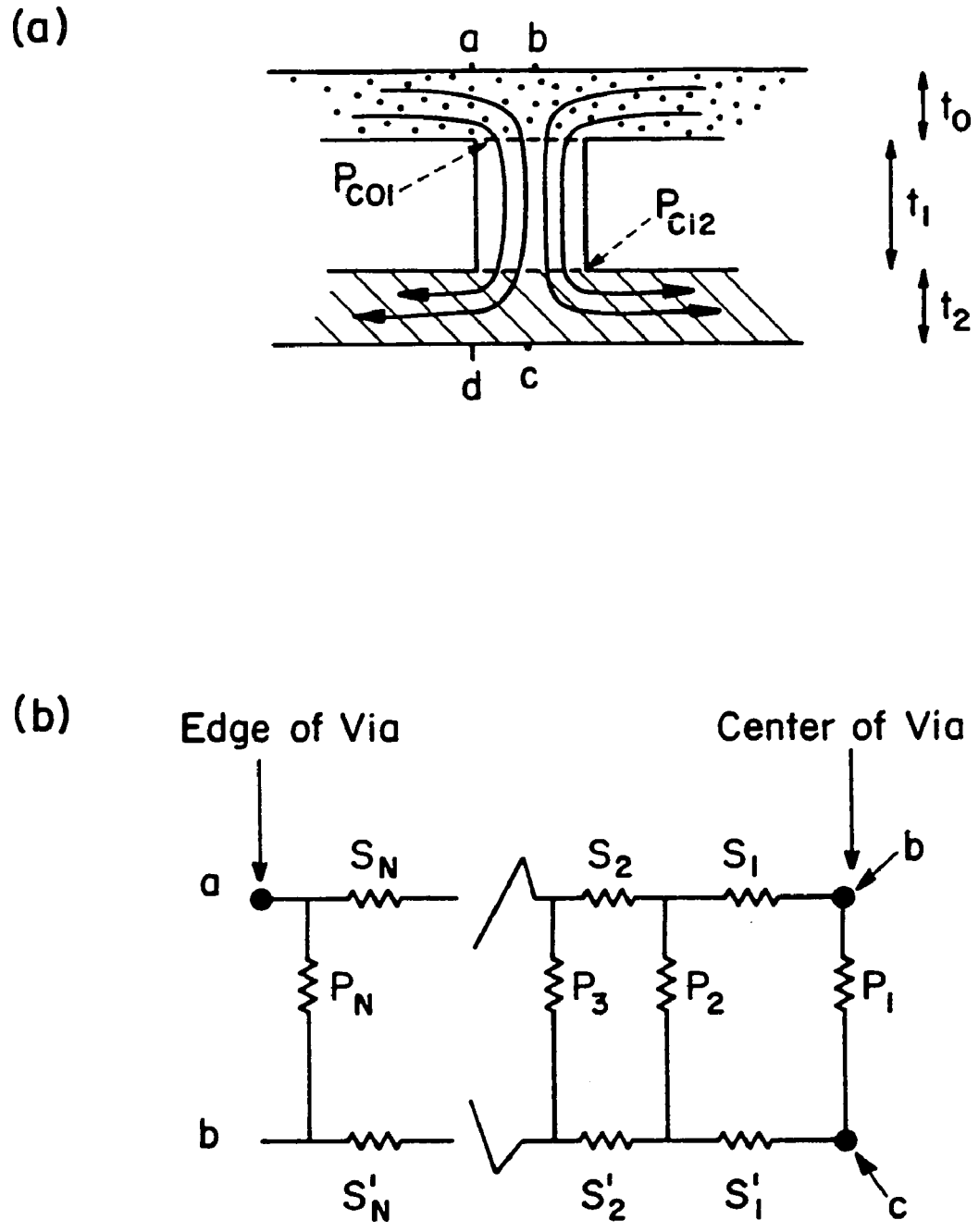

Figure 9.1 Current density distribution (a) in a via without current crowding. The equivalent circuit of a via from the edge to the center of the via is shown in (b).

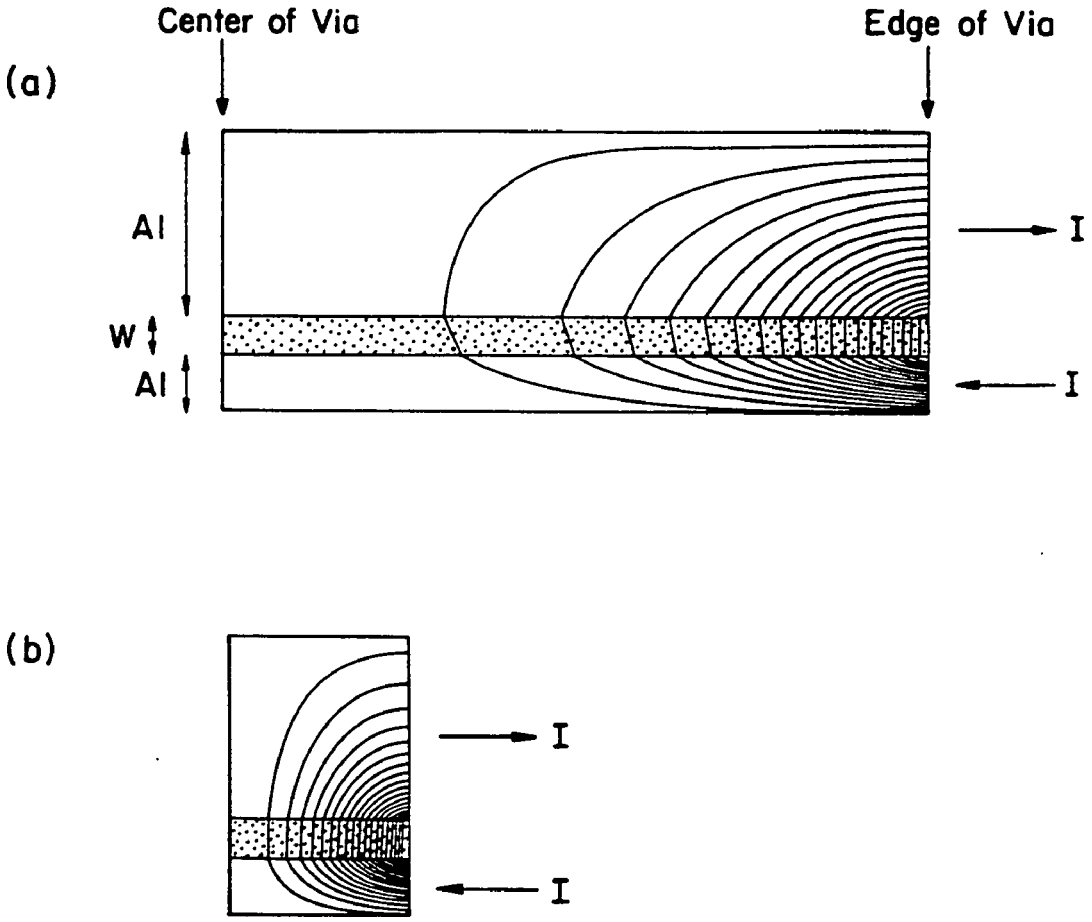

Figure 9.2 A cross sectional plot of the current density in (a) 5μm radius via (current crowding), and (b) 1μm radius via (approximately uniform current density). The data was obtained by 2-D numerical analysis. The Al(1.0μm)/W(0.2μm)/Al(0.3μm) structure had an interface (Al/W) resistivity of $P_c = 0.1\ \Omega\text{-}\mu m^2$.

Our objective in the following sections is to establish a simple analytical method for determining the correct value for P_c under any conditions of current crowding. Solutions which yield values for P_c were obtained for those vias which satisfy the thin film approximation.

9.3 Thin Film Approximation

We begin the analysis by assuming a structure with three layers and two interfaces (Fig. 9.1a). Furthermore we require that the layers of the structure be such that the effective "vertical resistance" along any vertical path through the via is due to the interface contact resistance P_{c01} and P_{c12}. A quantitative description of the thin film requirement is given as follows.

$$P_c \approx P_{c01} + P_{c12} >> R_{sho}t_o^2 + r_1t_1 + R_{sh2}t_2^2 \qquad (9.2)$$

P_c (Ω-cm^2)	the total contact resistivity
P_{c01}, P_{c12} (Ω-cm^2)	contact resistivity of the two interfaces
R_{sho}, R_{sh2} (Ω)	sheet resistance of the top/bottom layers
ρ_1 (Ω-cm)	resistivity of the plug material
t_o, t_1, t_2 (cm)	thicknesses of the layers

An equivalent circuit of this structure is shown Fig. 9.1b. The factors S_i are related to the sheet resistance of the layers and the P_i factors are related to the interface resistance. Our goal is to obtain values for the equivalent total resistance R_c of this network in terms of the values for sheet resistance (R_{sh}=R_{sho}+ R_{sh2}), interface resistance ($P_c = P_{c01} + P_{c12}$) and radius (a) of the via.

9.4 Analytical solution to current crowding at circular vias

The solution of the circuit shown in Fig. 9.1b will be given in terms of a equivalent resistance of the distributed network. To do this we analyze the circuit in terms of a differential equation. The vertical current density $J_z(r)$ is given by

$$J_z = V/P_c \tag{9.3}$$

where V(volts) is the vertical voltage difference across the top and bottom of the via. The horizontal current C(amps) is related to the derivative of the voltage ($dV/dr = V'$) by the following expression.

$$C = (2\pi r/R_{sh})\, V' \tag{9.4}$$

The vertical and horizontal current components are related through the continuity equation

$$C' = (2\pi r)\, J_z \tag{9.5}$$

where the derivative of the horizontal current is noted as $dC/dr = C'$. Combining Eqs. (9.3), (9.4) and (9.5), we obtain the differential equation

$$V'' + V'/r - V/L^2 = 0 \tag{9.6}$$

where $L^2 = P_c/R_{sh}$.

The solution of this equation can be written in terms of a zero order modified Bessel function $I_o(r/L)$.

$$V(r) = V(a)\, I_o(r/L) / I_o(a/L) \tag{9.7}$$

By using Eq. (9.4) we obtain an expression for the current C

$$C(r) = [2\pi r V(a)/R_{sh}]\ [I_o'(r/L)/I_o(a/L)] \tag{9.8}$$

in terms of the derivative of the Bessel function $dI_o/dr = I_o'(r/L) = [1/L]\, dI_o(q)/dq$. Since are goal is to obtain expressions for the (measured) equivalent resistance R_c

$$R_c = V(a) / C(a) \tag{9.9}$$

we can evaluate V(r) and C(r) at r=a with the result

$$R_c = [R_{sh}/2\pi a] [I_o(a/L)/ I_o'(a/L)] \tag{9.10}$$

Equation (9.10) represents the exact solution of the problem, which relates the measured parameters R_c, R_{sh} and "a" to the factor P_c. which is the main parameter of interest. Bessel[3] functions (and their derivatives) are cumbersome expressions to manipulate algebraically and they are usually expressed using polynomial functions with constant coefficients (α_i,β_i, etc.). For small values of r/L the function has the form,

$$I_o(r/L) = 1 + \alpha_1(r/L)^2 + \alpha_2(r/L)^4 + \ldots \tag{9.11}$$

And for large values of r/L the function can be written as

$$I_o(r/L) = (r/L)^{-1/2} \exp(r/L) [1 + \beta_1(r/L)^1 + \beta_2(r/L)^2 + \ldots] \tag{9.12}$$

By using Eqs. (9.10), (9.11) and (9.12), rearranging terms, and making the necessary approximations we obtain the first order approximation solutions to P_c.

The expression for P_c for small values of (r/L) is given as

$$P_c = F_s R_c \pi a^2 \tag{9.13}$$

where

$$F_s = 1\text{-}R_{sh}/(30R_c) \tag{9.14}$$

The term $30R_c$ in Eq. (9.14) was changed from $8\pi R_c$, which was derived from the first order approximation, in order to obtain more accurate values for P_c. Expression Eq. (9.13) is applicable over the range of

$$R_{sh}/R_c < 12.0 \tag{9.15}$$

For large values of r/L the contact resistivity P_c can be expressed as

$$P_c = (R_c 2\pi a F_B)^2/R_{sh} \tag{9.16}$$

where

$$F_B = 1\text{-}2.9R_c/R_{sh} \tag{9.17}$$

This solution is applied over the range

$$R_{sh}/R_c > 12.0 \qquad (9.18)$$

The term $2.9R_c$ in Eq. (9.17) was changed from πR_c, which was derived from the first order approximation, so as to increase the accuracy for P_c.

Together these approximate solutions estimate the value for P_C to within ≈2% of the exact value which can be obtained (with difficulty) from Eq. (9.10). To apply these solutions to a particular system, we first measure R_c, R_{sh}, and "a", then decide which solution is applicable (from Eqs. (9.15) and (9.18)), and then calculate the value for P_c with either Eq. (9.13) or (9.16).

To demonstrate the accuracy of these analytic solutions over a wide range of possibilities, we compare them with the more realistic two dimensional model of the contact via. The comparison was made on an Al/W/Al structure as shown in Fig. 9.3 with an interface contact resistivity of the Al/W and W/Al of 0.4 Ω-μm^2. For this particular structure, the thin film conditions (Eq. 9.2) are satisfied and therefore it is appropriate to use the analytical solutions. The numerical values for P_c in this case were obtained by numerically solving the Laplacian using a two dimensional mesh. In order to obtain the numerical results a computer program was designed. The numerical results were obtained by the author's collaborators[2]. Two dimensional plots of the current density for two particular vias are shown Fig 9.2. A comparison between analytic and numerical solutions is displayed in Fig 9.3 and show good agreement. Note also, the effects of current crowding for larger vias.

Although the analytical solution has been restricted to cases constrained by the thin film approximation , these solutions can also be used in more general situations. The motivation for the restriction is to simplify the mathematics of the problem, converting the problem from 2-dimensional

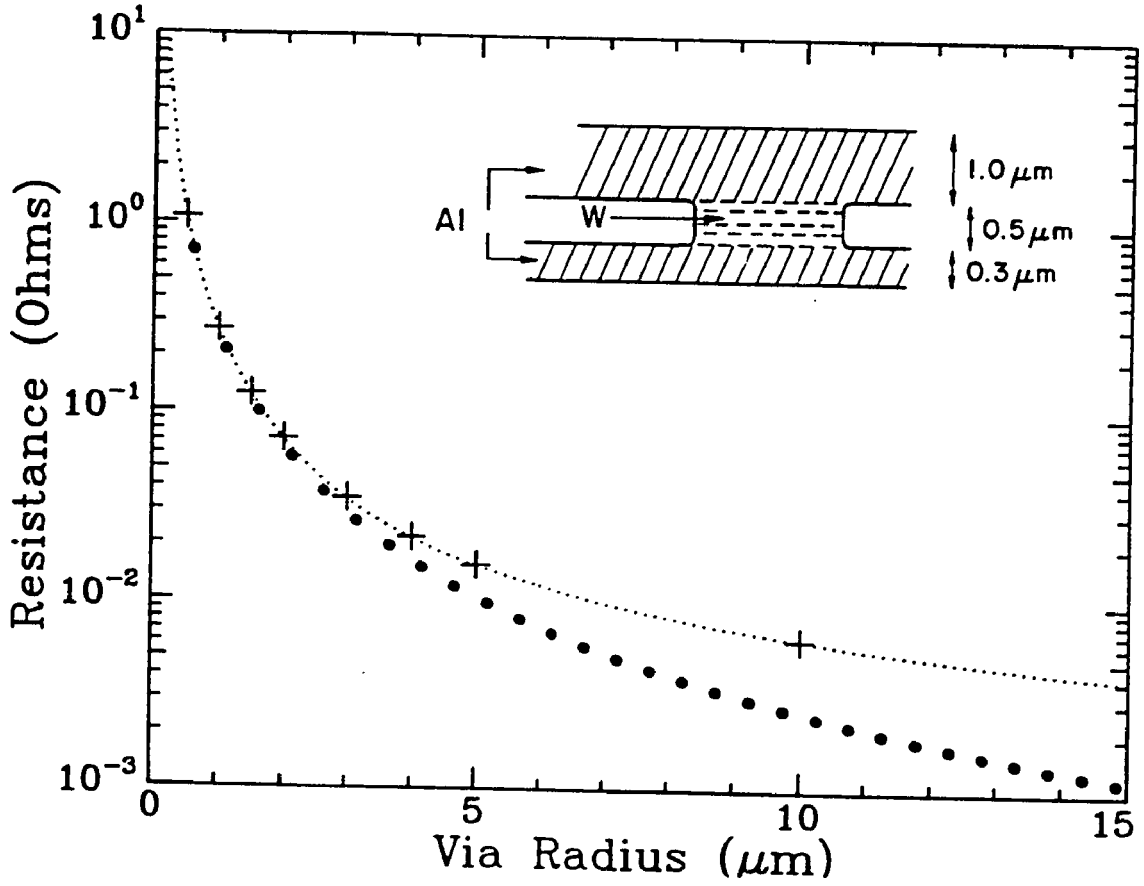

Figure 9.3 Comparison of contact resistance vs. via radius by 2-D numerical techniques(+) and analytical (solid line) solution from equations (9.13) and (9.16). Also shown is a plot (•••) of $R_c=0.07/\pi a^2$ where the effects of current crowding are not taken into account.

to 1-dimensional. A situation where the analytical solution can be modified slightly so as to circumvent the constraints of the thin-film approximation is as follows. Suppose the total (vertical) voltage difference in the via is not only due to the voltage difference at the interface, but incorporates the additional (vertical) voltage drop within the metal. In this situation the analytical solutions are used to obtain the value for P_C, but this value now represents a combination of interface and metal resistance. To approximate the correct value for the interface resistivity, the metal resistance is subtracted from the total resistivity $P_c(\text{interface}) = P_c - \rho_1 t_1$.

In summary, an analytical solution to the current crowding problem for circular vias with radially symmetric current has been obtained. The solution shows good agreement with the more rigorous numerical analysis.

9.5 References

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Chapter 10

Contact resistance study of selective tungsten CVD process on Al surfaces

10.1 Introduction

Selective CVD deposition of metals used in integrated circuits promises to be a viable technology for VLSI applications. Among the earliest candidates having success in many laboratories is the (WF_6) tungsten system.

This study investigates the initial attempts of depositing W on Al for a process in a startup operation[1] . The primary goal was to develop a contact resistance photolithographic mask set which would be used for diagnostic evaluation of the deposition process. In this chapter six samples of a startup operation will be discussed. The W/Al interface of the samples is analyzed with both electrical and material characterization techniques.

This study is not so much an investigation of the process of the deposition of W on Al but a study of a characterization technique of the deposition process. In fact deposition of W on Al using CVD processes has been done successfully by other workers[2] using a variety of CVD systems.

10.2 Experimental

Samples were fabricated on Si substrates which were thermally oxidized to form a buffer SiO_2 layer between the substrate and the subsequent metal layers. The contact resistance devices required a three mask (level) metallization scheme. A schematic of the process sequence is outlined in Fig. 10.1.

Using photolithography and the liftoff technique, patterns of 3000 Å Al or Al(Cu) were electron beam deposited onto the SiO_2 layer to form the bottom metal layer - which will be referred to as the M0 metal layer. These patterns were configured for Kelvin and spreading resistance structures for the purpose of measuring the contact resistance.

Following the bottom metallization , SiO_2 was sputtered onto the samples in order to form an isolation layer between levels M1 and M2 metal layers. Vias of sizes ranging from 3 to 700 μm^2 were etched through the SiO_2 layer using the reactive ion etching process.

Prior to loading in the W CVD system the samples were cleaned with HCL, this system did not allow for in-situ cleaning before deposition. Six samples were fabricated with the CVD W machine over a wide range of process parameters, including various temperatures (330-550°C), deposition times, and process gases (SiH_4, H_2). This middle level (of W metallization) will be referred to as level M1. A log of these different process conditions are given in Table 10.1

After W deposition, the final level M2 of Al (1μm) was deposited using the liftoff technique in a pattern useful for Kelvin and spreading resistance measurements. These samples were in-situ sputter cleaned prior to the E-beam Al deposition to insure an oxide free surface.

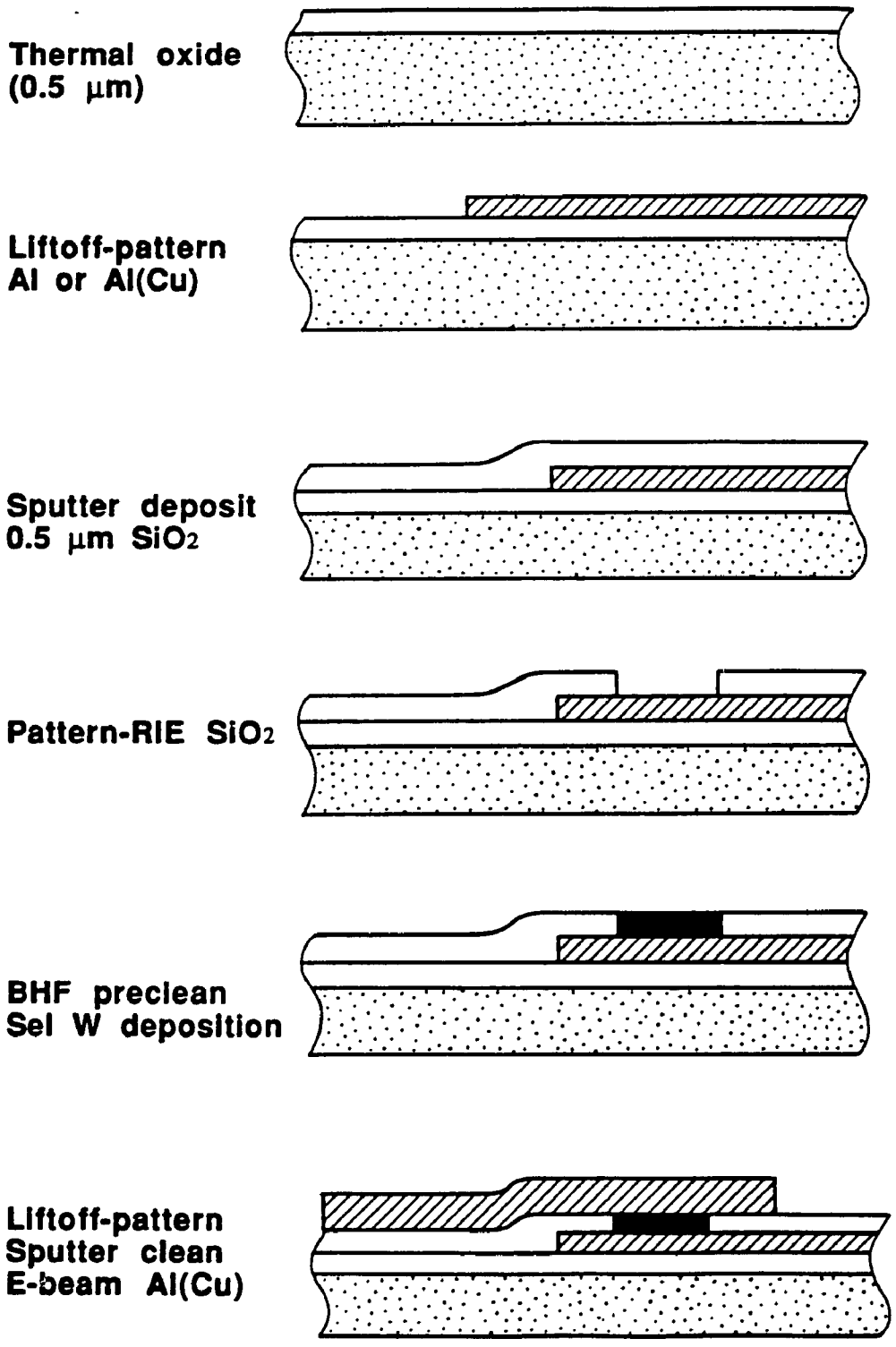

Figure 10.1 Sequence of process steps for contact resistance devices.

10.3 Electrical characterization of via contacts

After final processing of the samples, they were characterized by measuring the contact resistance of both Kelvin and spreading resistance structures. The results, shown in Fig. 10.2a, are the values of contact resistivity values Pc, which represent the contact resistance normalized for the area of the via. Note the wide variation in the values, ranging over 5 orders of magnitude.

The contacts for the small vias of size less than 10 μm^2 were blocking (Rc >20 MΩ) and thus couldn't be measured. These blocking contacts could be irreversible changed ("punched through") subsequently reducing the resistance from $R_c > 20M\Omega$ to $R_c < 10\Omega$ by applying voltages of greater than 2 V (Fig. 10.2b). Also shown in Fig.10.2c is the voltage breakdown characteristics of the SiO_2 layer obtained using a contact pad having a zero via size. The resistance does not linearly scale with area.

It is deduced from these data that there is a thin layer of electrically insulating material within the contact limiting the current from the top (M2) to the bottom (M0) metal layers. The origin of this layer will be investigated in a following section. It is speculated that this layer is continuous for small areas (<5 μm^2) accounting for blocking contacts, but for the larger areas (>50 μm^2) there are discrete pin-holes through the insulating layer allowing current conduction between the levels. From this we calculate the density of these pin holes to be on the order of 1/50 μm^2.

Given that this high resistance insulating layer exits, it is imperative to identify the location of the layer. It is assumed that the layer is associated with the interface. Since there are two interfaces in the stacked via , it is possible that the insulting layer be associated with either M0/M1 or M1/M2 interface as shown in 10.4a. Determining which interface is responsible

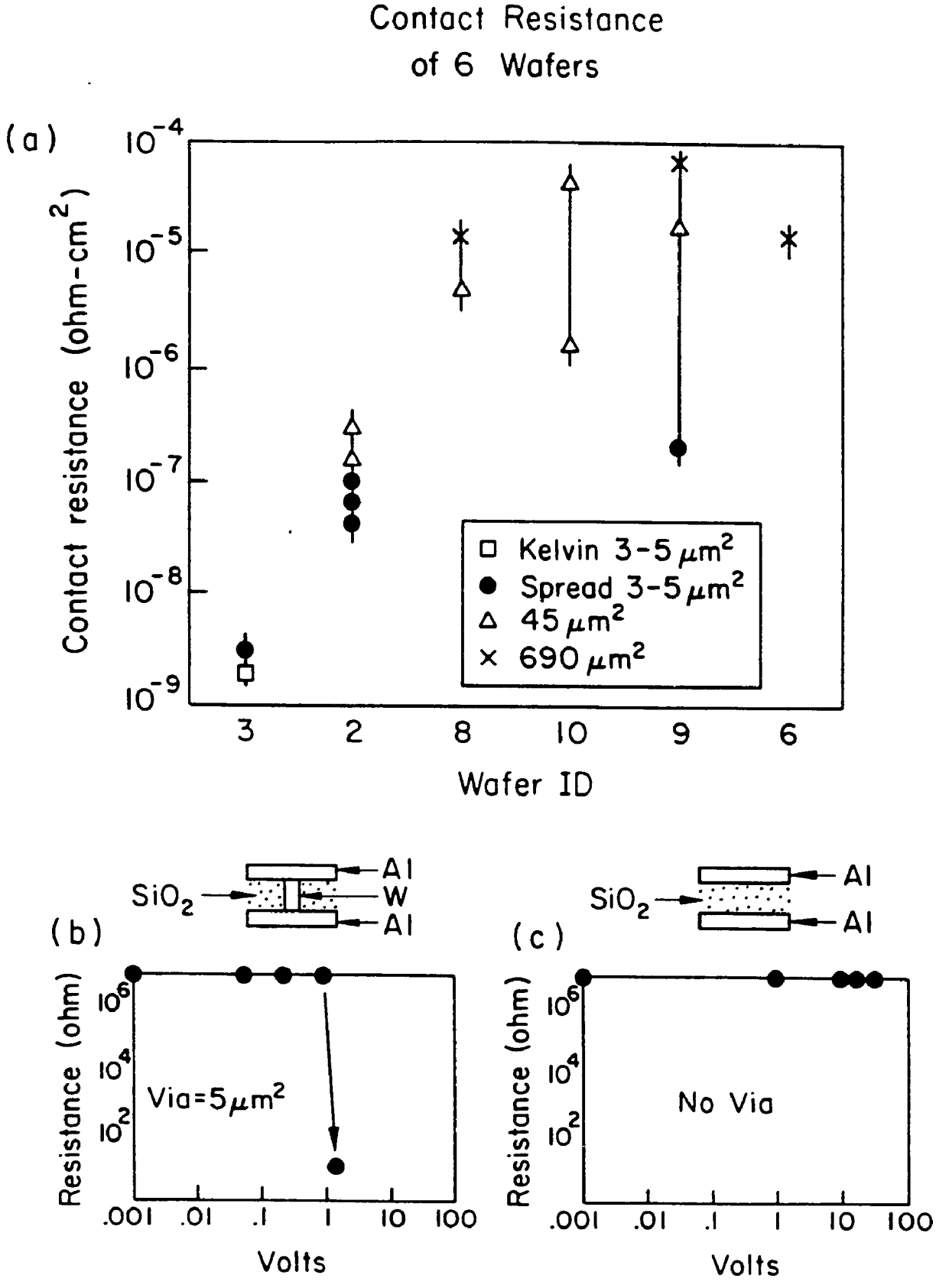

Figure10.2 (a) Contact resistance of six wafers and voltage breakdown of (b) small vias and (c) oxide layer of the high resistance samples.

can be accomplished by an electrical measurement using structures on the wafer which were specially designed for these type queries. From the previous paragraph it is known that the contact resistance is strongly dependent on the area of the interface. By comparing the total contact resistance between vias which have differing M0/M1 and M1/M2 interface areas it is possible to deduce which contact is blocking.

Compare the structures in Fig. 10.3b and Fig. 10.3c. The M1/M2 interface area is the same for both structures, whereas the M0/M1 interface is 20 times the area for the structure in Fig. 10.3c. Since the resistance of the structure in Fig. 10.3b is found to be greater than 10^6 that of the structure in Fig. 10.3c, it is deduced that the insulating layer which causes the high resistance is located at the M0/M1 interface. This interface is associated with the exposed Al surface prior to growth of W occur. In order to further investigate the origin of the insulating layer material characterization tools are used including SEM and Auger.

10.4 Material characterization of via contacts

The samples were examined by SEM inspection and an unexpected result was found: samples which had low contact resistance were not filled with W and in some cases had only little W in the via. A comparison of samples 3 and 8 in Fig. 10.4 show the contrast between the filled via (high resistance sample 8) and the low partially filled via (low resistance sample 3). The bright contrast nodules in the vias (Fig. 10.4) were identified as W using with wavelength-dispersive-spectroscopy (imaging mode)

Further analysis, using energy-dispersive-spectroscopy in the focused beam mode, shows (Fig.10 5) that the W layer in the unfilled via is not

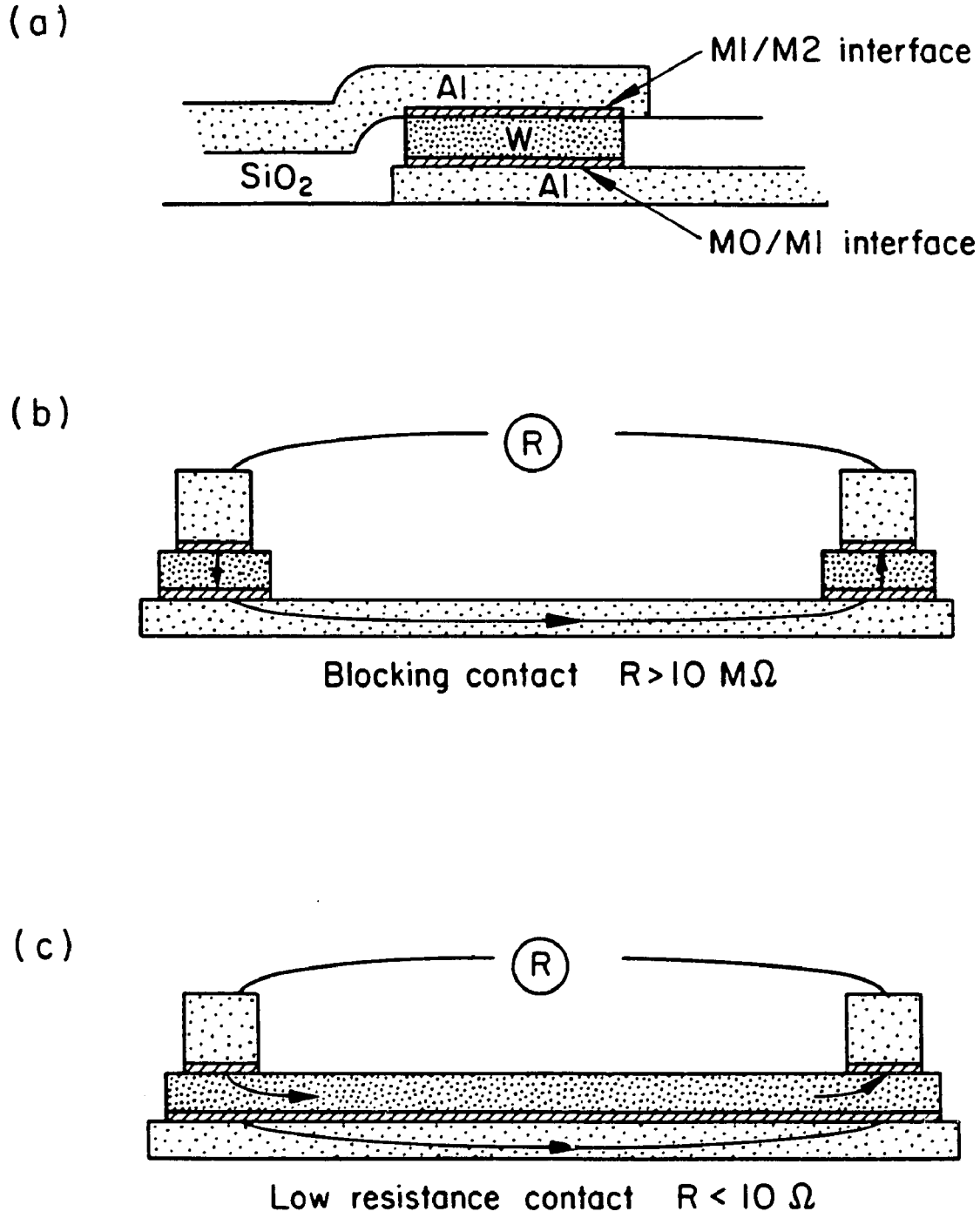

Figure 10.3 (a) Diagram of Al/W/Al contact resistance structures where the two interfaces have the same (b) and different(c) areas.

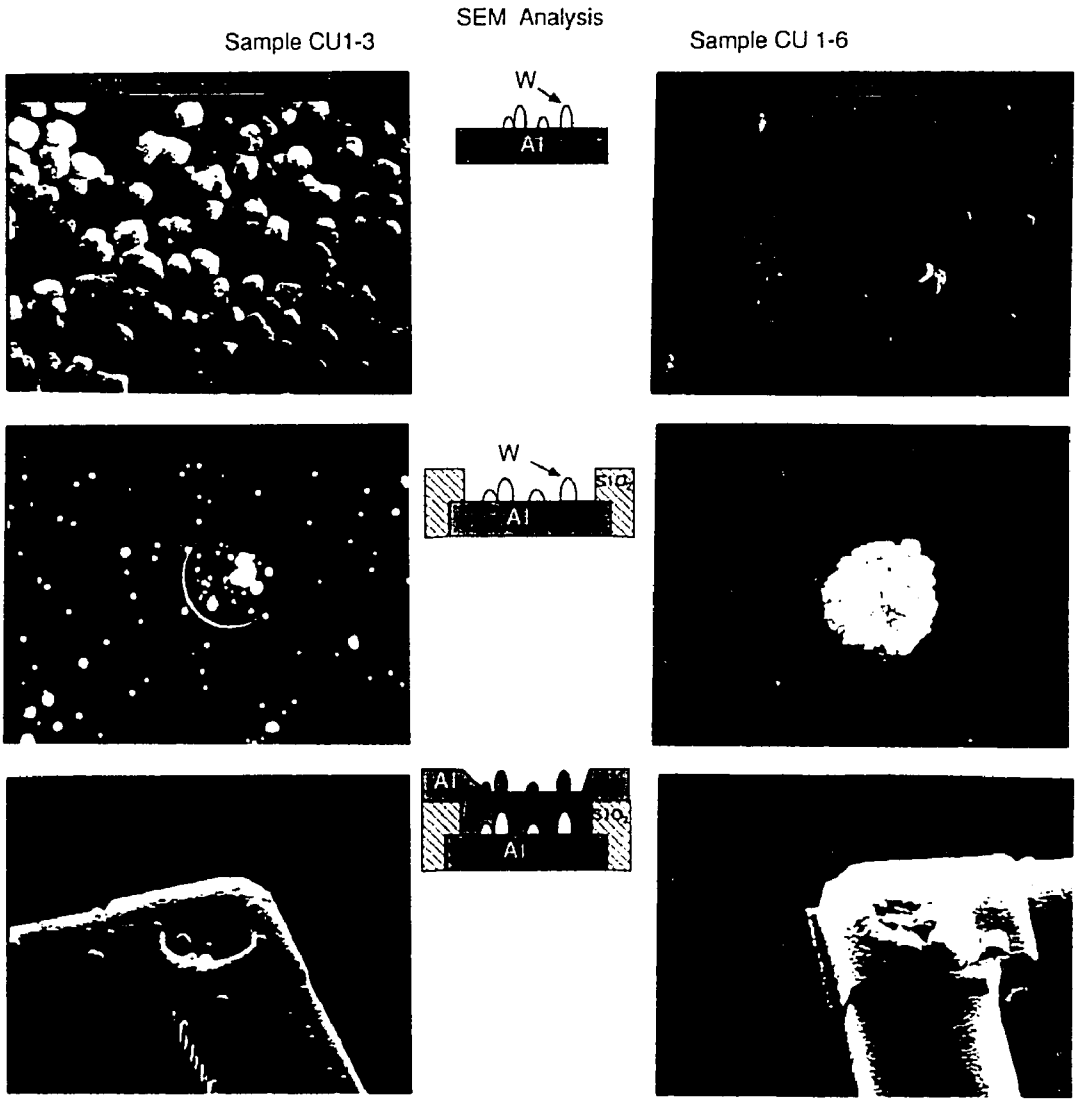

Figure 10.4 SEM micrographs of low resistance/unfilled via (left column) and high resistance filled via (right column).

(a)

(b)

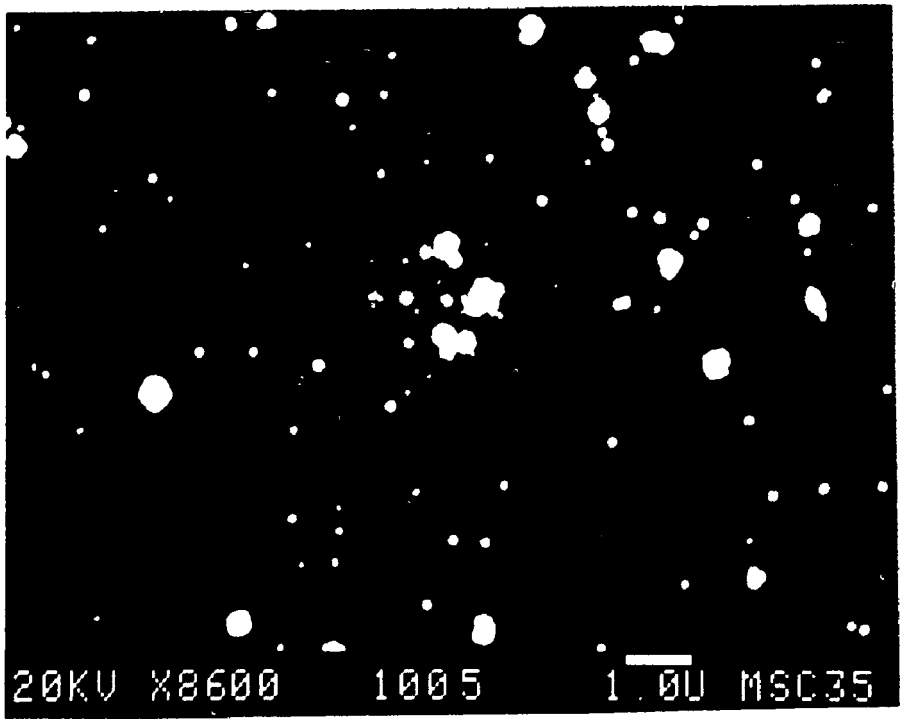

Figure 10.5 Micrographs of via (low resistance) sample using (a) imaging wavelength dispersive spectroscopy and (b) SEM.

laterally continuous. By comparing different structures on the same wafer it is possible to show the W layer before (Fig. 10.6.a) and after (Fig. 10.6.b) final Al metallization (M2). It is concluded that in the case of the low resistance sample, the top Al layer (M2) is in direct contact with the bottom Al layer (M0), the current being shunted around the W nodules (islands) through the Al.

To obtain more information about the (speculated) insulating layer, Auger electron spectroscopy (AES) was used on sample structures which did not have the top Al layer. This data was taken by Lynn Rathbun. The data shown in Fig. 10.7 indicates that oxide and fluoride compounds and carbon are present on the Al surface in places where the W did not grow. Since this surface was exposed to the ambient air after taking the samples out of the deposition reactor, the source of these contaminating compounds can not be traced. Was the Al surface contaminated before, during or after the W deposition process? Because in-situ surface analysis was not done during the deposition the source of the contaminants can only be speculated.

10.5 Discussion and conclusions

Electrical and material characterization of the six samples in this study showed that some of the samples had high contact resistance due to an insulating layer at the bottom Al/W interface. Since all the samples with complete W coverage (filled vias) show the highest resistance, resulting from the insulating layer, it is concluded that this insulating layer was formed prior to and/or in the initial stages of the W deposition.

The oxide compounds, including Al_2O_3, are likely to be present prior to deposition due to the native oxide on the Al. The oxygen can easily be

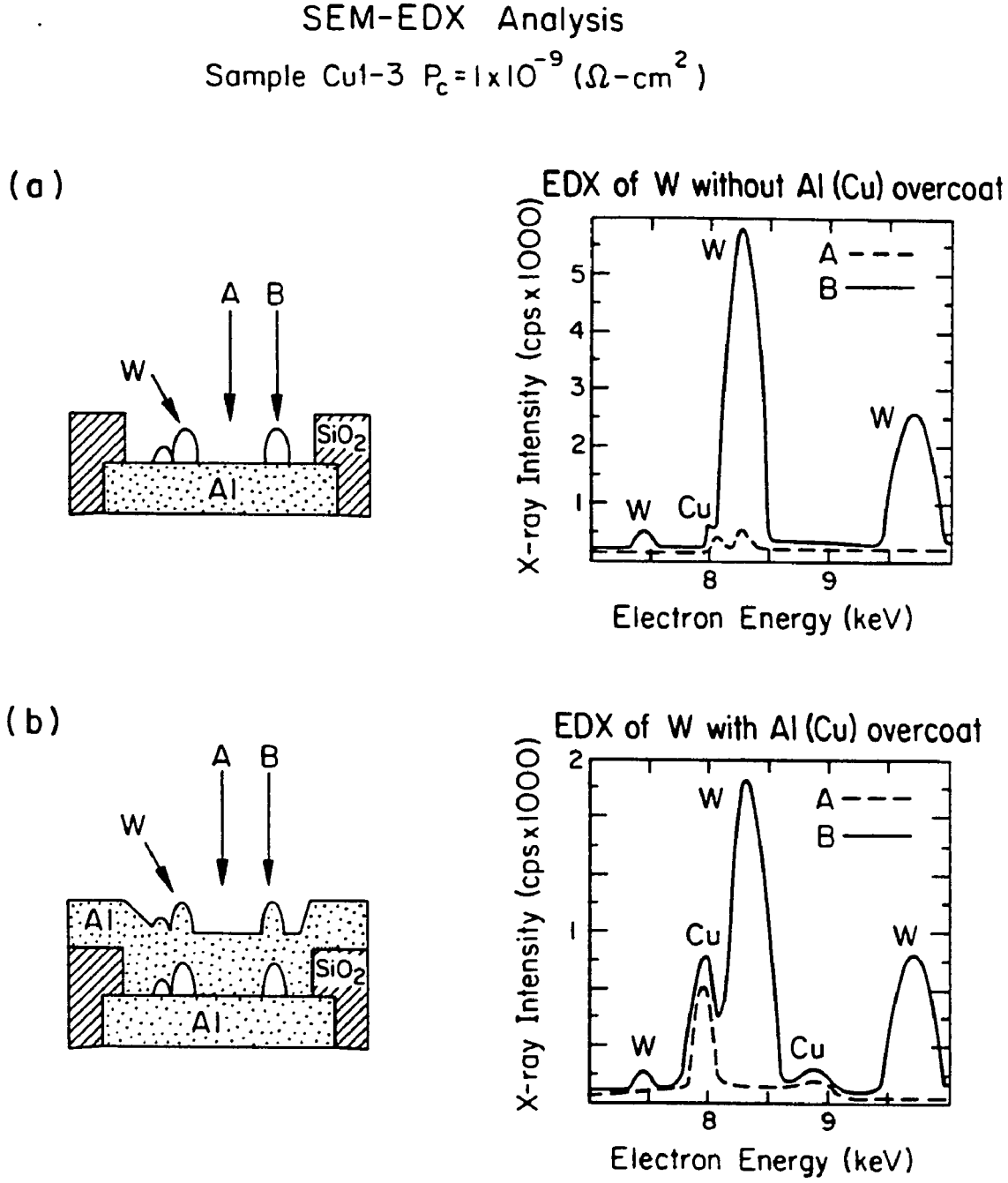

Figure 10.6 SEM-EDX analysis of low resistance sample with (a) and without (b) the final 1 μm Al metallization.

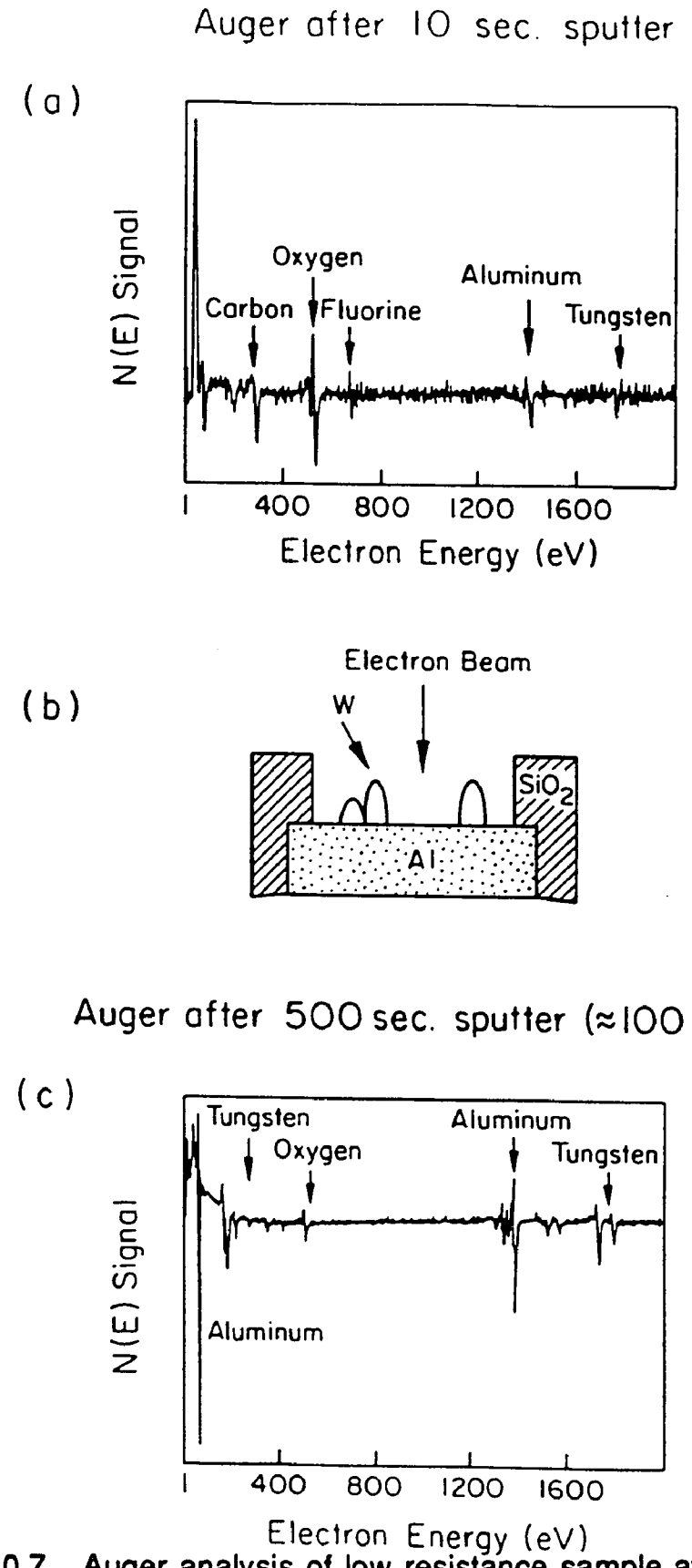

Figure 10.7 Auger analysis of low resistance sample at a location on the sample where W did not seed shows F,C, and O at the surface.

supplied prior to sample loading and during the initial heat-up stages of deposition (from the walls of the reactor[3]). It has been shown that W deposition will be suppressed by only 5 nm of Al_2O_3, allowing only a few isolated grains of W to grow[4].

Nonvolatile fluoride compounds such as AlF_3 could be generated during the initial stages of the W deposition[2] before the reaction between the (deposited) W and WF_6 is self sustaining.

The carbon on the surface (identified from Auger data) could be in the form of insulating polymer compounds, formed prior to the W CVD deposition during the SiO_2 (RIE) etching process. Polymer compounds have been shown to be formed on the surface during etching (RIE) of SiO_2 if CF_4 (gas) has been used. Apparently the polymer film forms at the end of the etching process when there is no more SiO_2 remaining, which allows a competing reaction to dominate - the breakdown of the CF_4 to form polymers.

In all cases the insulating film at the interface produces two undesirable effects: it inhibits nucleation of the W grains and produces a high resistance interface barrier which yield the contact useless for interconnects. Tungsten grains do nucleate even on the contaminated surface. This is possibly due to small pinholes in the insulating layer, which may also act as (current) shunting paths through the insulating layer. After nucleation of the W grains, lateral growth occurs until impingement of adjacent grains occurs, thus completely covering the insulating layer. A model of this speculated process is shown in Fig. 10.8.

One problem with the model concerns the low resistance sample which was analysed in the previous sections. This sample has limited W deposition but low contact resistance. For the other high contact resistance samples, this layer acts as a high resistance barrier to current. It is assumed

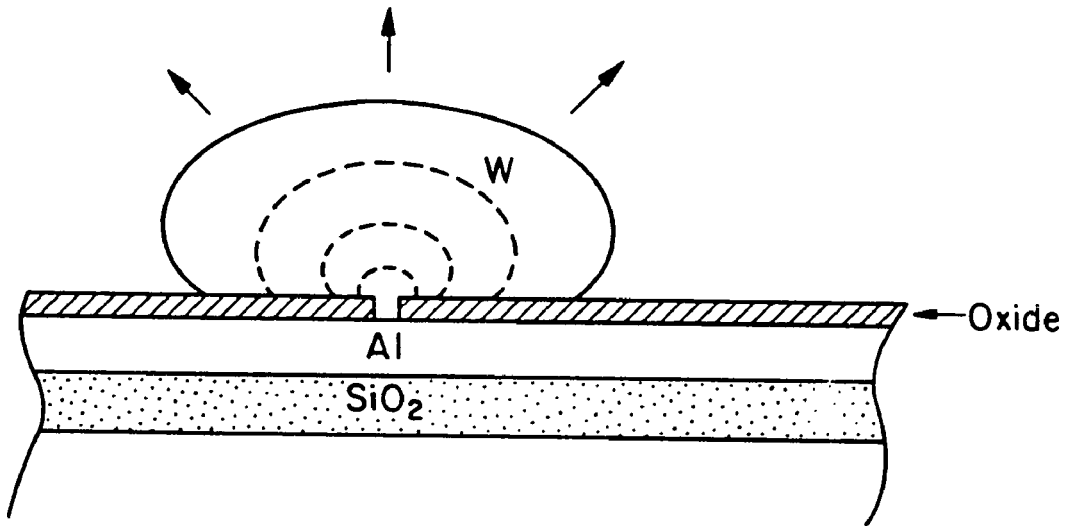

Figure 10.8 Model of W nucleation and growth on an electrically insulating (contaminated) surface layer with pinholes.

that this layer was also present during the deposition for the low resistance sample. From the earlier discussion this sample has the top Al layer connected to the bottom Al layer. The question is, what happened to the insulating layer for the low contact resistance sample? This layer was most likely was removed during the top Al metallization process because all samples are in-situ sputter cleaned prior to e-beam deposition of Al. To verify this idea samples were formed without the CVD W process yielding Al/Al interfaces. Samples formed using the top metallization process without the in-situ sputter clean had high contact resistance (R>20 MΩ) whereas the in-situ cleaned samples had low resistance (R<10Ω) contacts. It is suggested that a similar in-situ cleaning process be designed into the new generation selective tungsten machines.

10.6 References

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Chapter 11

Ohmic contacts to *n*-GaAs using Pd/In metallization

11.1 Introduction

In this chapter the reaction between indium/palladium and GaAs is discussed. The metal/semiconductor interface is important because it controls the resistance of the device, it determines whether the I-V characteristics are ohmic or diode-like. And like the W/Al interface the initial contamination layer (oxides) is also important, but the critical factor in this section regarding the formation of ohmic contacts is the reacted interface layer, created by thermally annealing the sample. New compounds are formed at the interface as the result of the reaction between the metal and semiconductor. Although the initial oxide layer does effect the reaction, it is the formation of the new compounds at the interface which is if most interest, since it lowers the contact resistance at the interface by typically >6 orders of magnitude. The contact resistance measurement provides a sensitive albeit indirect tool in the study of interfaces.

Ohmic contacts to n-GaAs are conventionally made with a Au-Ge metallization[1] by thermally annealing the sample above the Au-Ge eutectic point. The initial Au-Ge/GaAs interface, as in the case of most metal, forms Schottky diodes with typical barriers heights of $\phi \approx 0.8$ eV (Fig. 1a). During annealing, the alloy interacts with the GaAs and forms a low resistance

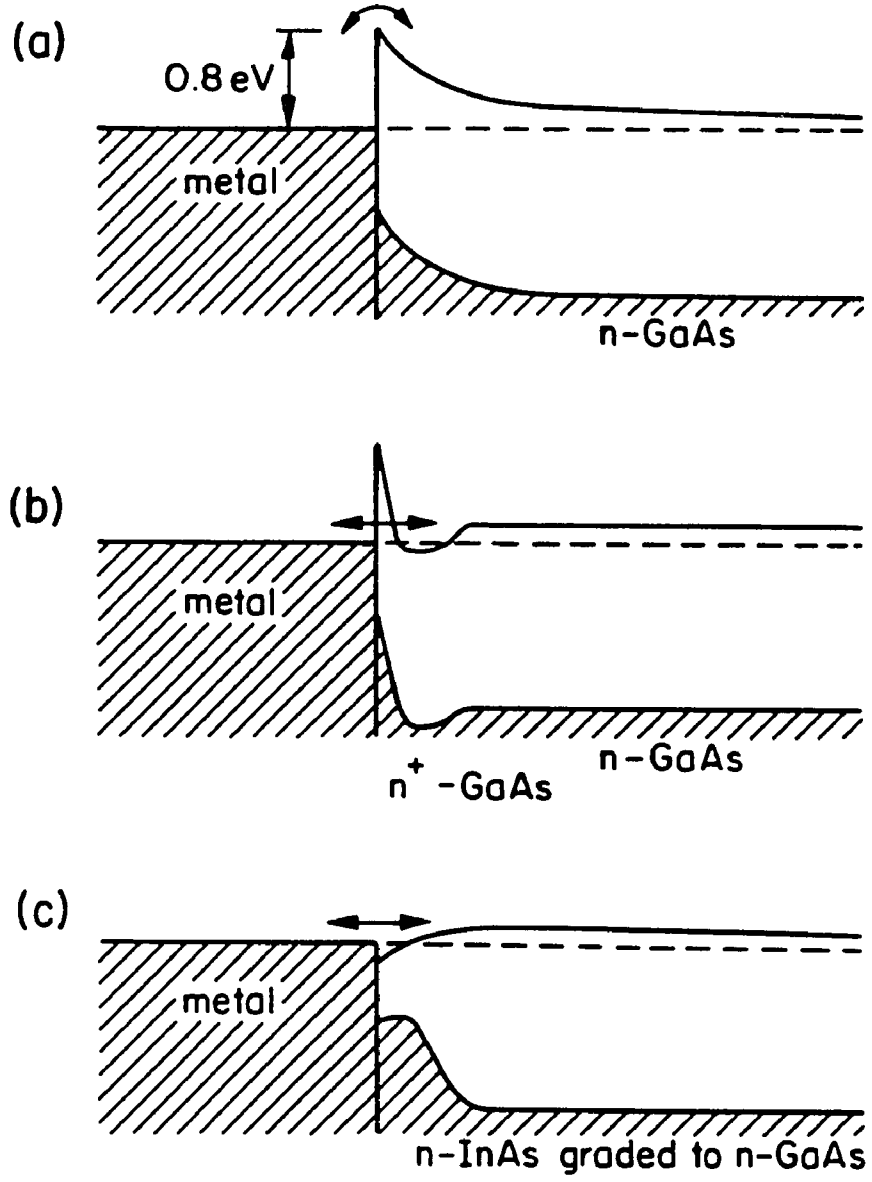


Figure 11.1 Band diagrams for metal on (a) medium doped GaAs (Schottky diode) showing typical 0.8 eV barrier height, (b) highly doped GaAs which shows tunnelling through the barrier resulting in low resistance and linear I-V characteristics, and (c) a modulated bandgap $In_xGa_{1-x}As$ having a reduced barier height.

contact, possibly due to tunnelling through the barrier to the highly doped GaAs region near the contact (Fig. 1b).

This (Au/Ge) process has two major shortcomings. The first problem relates to the morphology of the metal/GaAs interface, the reaction occurs in the liquid state and leads to localized reactions resulting in spiking into the substrate. These spikes can not be tolerated in some devices which have shallow, multi-layer structures. The second problem for the Au/Ge contacts is common for all tunnelling type ohmic contacts, that is, the value of contact resistance ultimately depends on the doping level of GaAs substrate, the higher the doping the lower the resistance. However, GaAs has an apparant upper limit to which it can be doped with Si. Higher concentrations can be implanted into the substrate,but the concentration of activated sites is limited to values on the order of 10^{18} cm^{-3}. the standard doping.

In order to circumvent these problems we investigated contacts using a solid state reaction at the interface in order to reduce interface morphology problems. We also used the idea of bandgap engineering, whereby we form compounds the interfacecrearting a graded-bandgap junction rather than the tunneling type junction.

Uniform ohmic contacts to n-GaAs have been fabricated with graded $In_xGa_{1-x}As$ layers[2] (Fig. 1c) and abrupt InAs/GaAs interfaces[3] ($\rho_C \approx 1 \times 10^{-6}$ Ω-cm^2) grown by molecular beam epitaxy (MBE). However, MBE techniques do not allow the use of photoresists for pattern definition during deposition. Alternatively, more conventional techniques have been used including thermal evaporation of indium onto GaAs substrates producing contacts with resistance values of $\rho_C \approx 1 \times 10^{-5}$ Ω-cm^2. As in the case of the AuGe system, the reaction occurred in the liquid state which again produced

morphology problems at the interface. Improvements[5] in the interface morphology were made by adding a thin layer of Pt (400Å) between the In and GaAs. This decreased the contact resistance to 2×10^{-6} Ω-cm^2.

Another type of contact currently being investigated is the Ge/Pd/GaAs structure[6,7]. This system forms a non-alloyed, uniform contact with resistance values of 1×10^{-6} Ω-cm^2. The initial reaction between Pd and GaAs forms a Ga rich Pd_xGa_yAs compound at the interface[8].

In this chapter we discuss the results[9] of our study of ohmic contacts to *n*-GaAs using an In/Pd metallization where the goal is to form shallow graded-bandgap junction which are ohmic.

11.2 Experimental

Palladium(400Å) and indium(4000Å) were sequentially evaporated with an electron beam deposition system (base pressure of 1×10^{-8} Torr) producing an In/Pd/GaAs structure. Layers were deposited at a rate of ≈ 5Å/sec. The GaAs substrate material included both bulk Si-doped n-GaAs ($N_d \approx 5 \times 10^{17}$ cm^{-3}) and a Si-doped epilayer grown by vapor phase epitaxy on semi-insulating GaAs. The epilayer consisted of a top layer (1800 Å thick) with nominal Si-doping of 2×10^{18}cm^{-3} and a lower layer (4000Å thick) with Si-doping of 2×10^{17}cm^{-3}.

Electrical measurements were performed using the transmission line mode (TLM)[10] method and the method of Cox and Stack[11]. In both cases samples were patterned with photoresist prior to deposition. Those samples used for TLM measurements were first etched to form a mesa 100 μm wide with depth of ≈1 μm. The contact pad spacing for the TLM pattern

ranged from 5 μm to 40 μm. The diameter of the dots used in the Cox and Strack method ranged from 9 μm to 100 μm. Final surface preparation included an etch in a 1:1 HCl/H_2O solution followed by an etch in a 1:15 NH_4OH/H_2O solution. After deposition the excess metal was lifted off by soaking the samples in acetone.

The samples were annealed using a Heatpulse™ 410 flashlamp rapid-thermal annealer (RTA). The system was purged (20cc/sec) during annealing with either Ar/H_2 (9:1) or N_2. At 500°C the heating and cooling rate of this system was 90°C/sec and 10°C/sec respectfully.

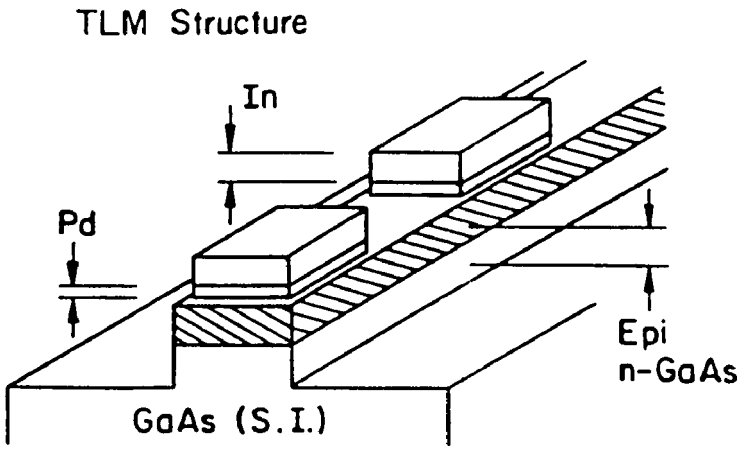
Material analysis was made using 2.8 MeV $^4He^{++}$ Rutherford backscattering spectrometry (RBS) and Auger electron spectroscopy (AES). X-ray diffraction measurements were taken with a Guinier camera and Scintag™ diffractometer using Cu $K\alpha$ radiation. The interface was examined in cross-section by transmission electron microscopy (TEM) with a JEOL 4000™ microscope operating at an accelerating voltage of 400 keV and by scanning electron microscopy (SEM) using a Cambridge S200™.

11.3 Electrical measurements

As expected the unannealed metal/semiconductor contacts showed rectifying (Schottky diode) I-V characteristics. After annealing at 500°C for 20 sec. the contacts showed linear, low resistance I-V characteristics. To obtain the values for the specific contact resistivity, the resistance between adjacent contact pads on the TLM pattern was measured and plotted versus the pad spacings. A least squares fit was applied to the resistance - pad spacing data and the transfer length $L_t = L_x/2$ (L_x = intercept at R = 0 in Fig.2)

and sheet resistance R_{sh} (slope of the line in Fig.2) were extracted. A value for ρ_c was evaluated by the relation $\rho_c = L_T^2 R_{sh}$. Four samples annealed separately under either N_2 or Ar/H_2 ambients gave values for ρ_c of 1.5, 1.1, 0.76 and 0.67 $x10^{-6}$ Ω-cm^2. Additional measurements on contacts to bulk doped substrates using the method of Cox and Stack verified that the resistance values were in the low 10^{-6} Ω-cm^2 range.

Thermal stability of these contacts was tested by continuous annealing the samples at 400°C using the RTA system at 5 min intervals for an accumulated time of 30 min. The resistance of the contact increased from 1.2 to 2.8 $x10^{-6}$ Ω-cm^2 (Fig. 3).



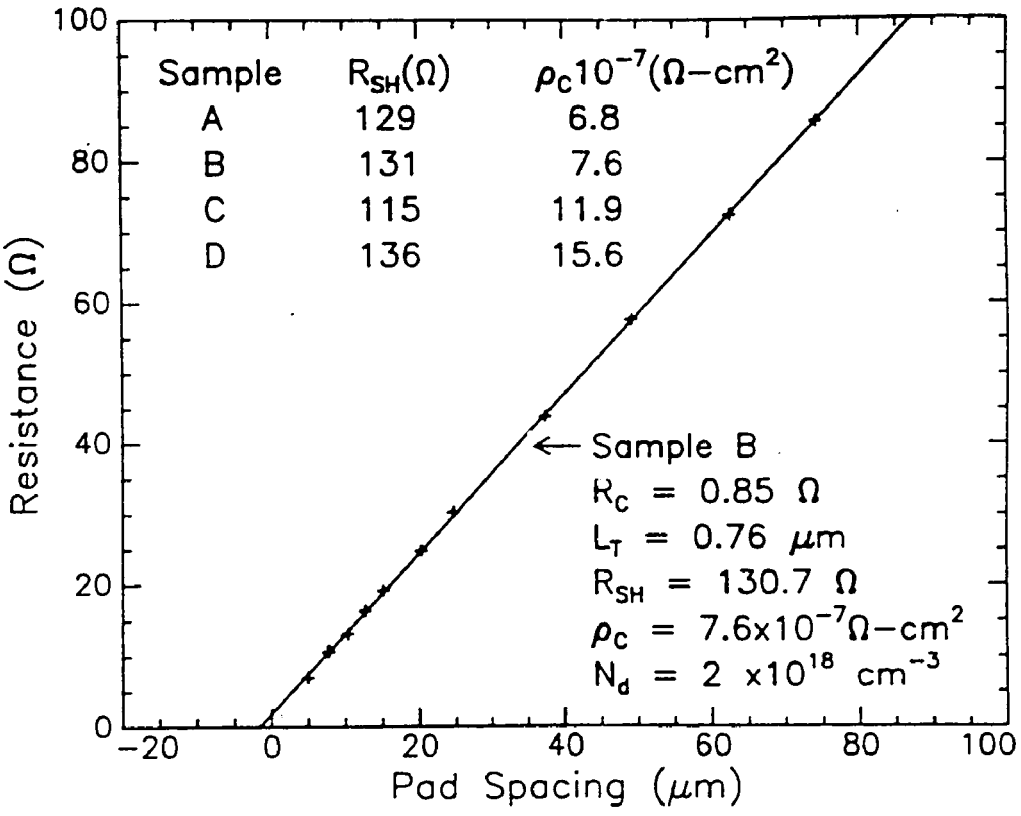


Figure 11.2 TLM data for In/Pd contacts annealed at 500°C for 20 sec.

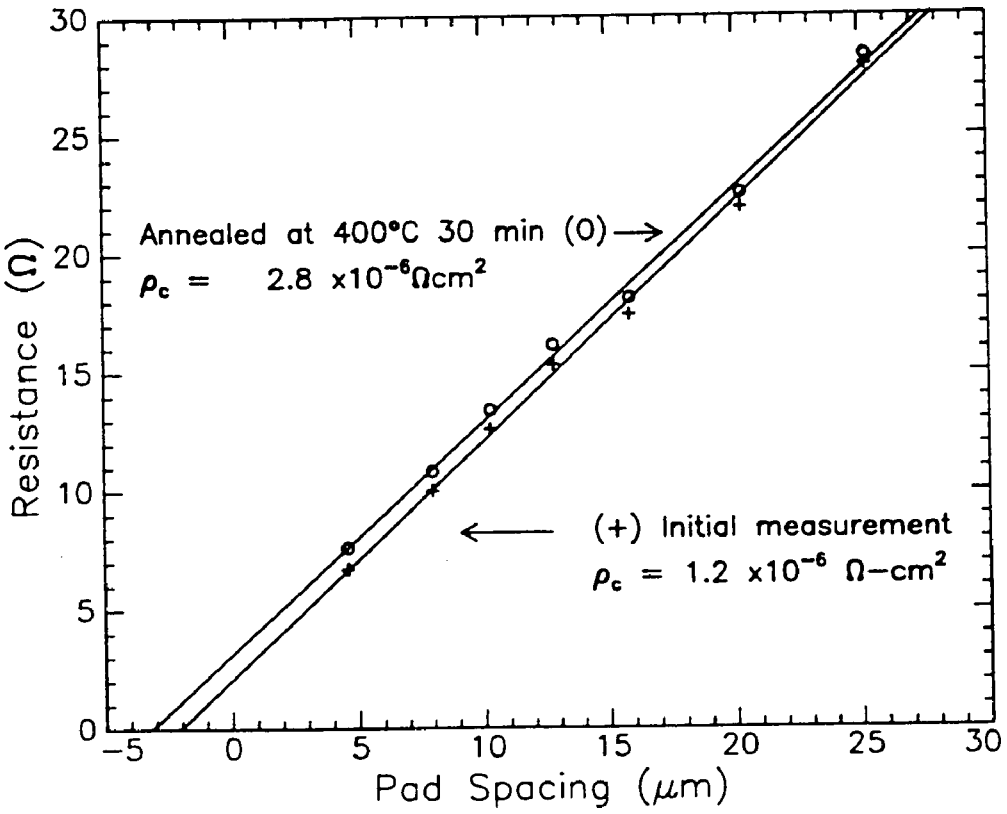


Figure 11.3 Thermal stability of contacts. Resistance measurements taken before and after 400°C 30 min anneal.

11.4 Material characterization

The top indium layer was laterally nonuniform before and after annealing as verified by plan-view and cross-sectional SEM photographs. This was expected since the melting temperature of In is ≈ 155°C. Cross sectional TEM micrographs of the interface shown in Fig.4 indicate that the metal/GaAs interface is laterally uniform and that a thin ≈ 200-500 Å reacted region had formed.

This interface was also probed via SIMS analysis. Because the morphology of the top surface of the sample is nonuniform front side depth profiling would not be very useful. So the technique of the back side depth profiling was used. Samples were analysed by Chris Palmstrom at Bellcore Corp, the place where the technique was developed. Special samples were made which consisted of an epi GaAs layer grown on an intermediate Al-GaAs buffer layer, a GaAs substrate acts as a carrier substrate for the layers. After metallization and annealing the thin GaAs, reacted layer and metal film are removed intact from the supporting substrate using a special processing technique.supports the layer. The results given in Fig 11.5, show that the transition between the GaAs an metal layers is rather abrupt, changing over a 500 Å region. The leading tail on the indium curve is attributed to microcracks in the film and not to the indium concentration in the bulk GaAs.

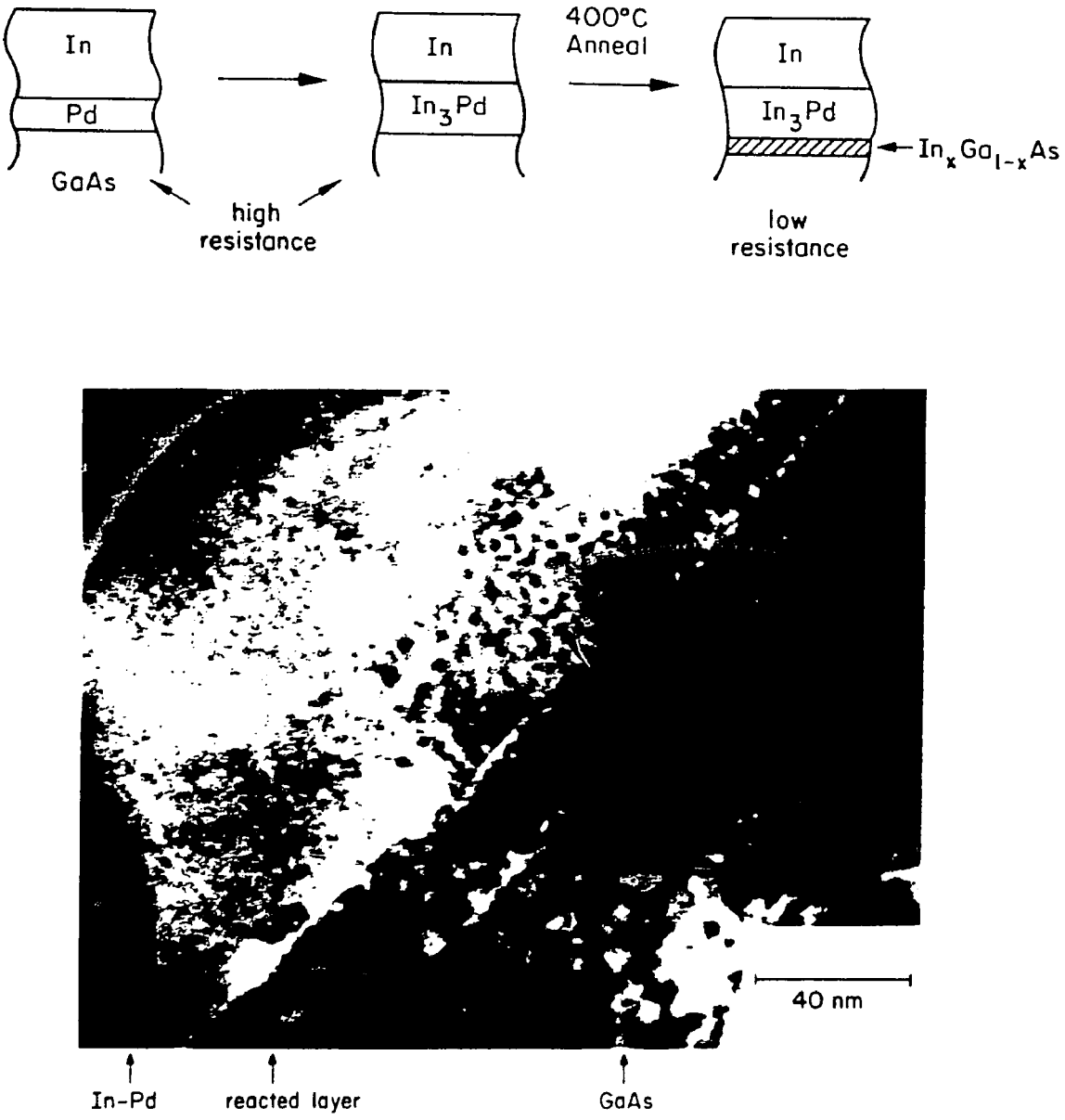


Figure 11.4 Bright field transmission electron micrograph of a [110] cross-sectional view of a In/Pd/GaAs sample after an anneal at 500°C for 20 sec and proposed sequence of the formation of compounds.

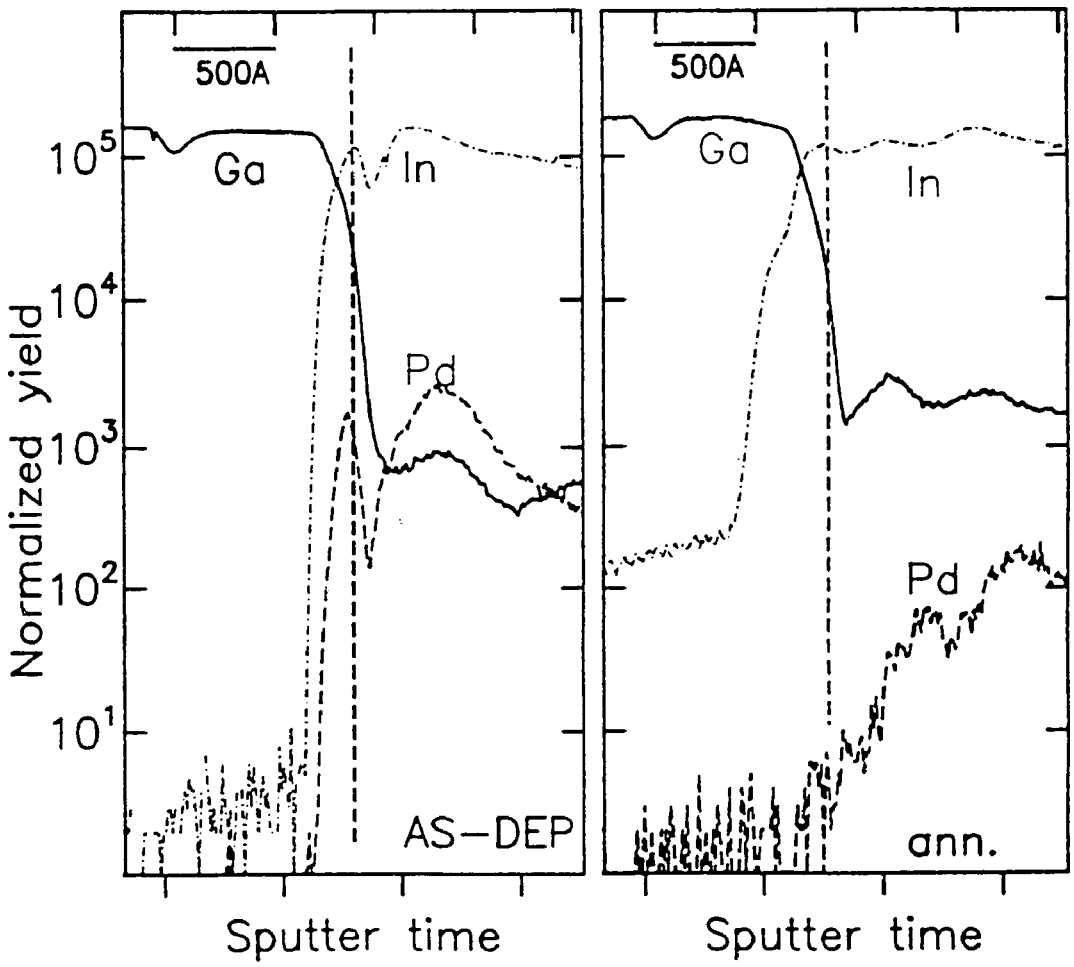


Figure 11.5 Backside SIMS depth profile of (a) as-deposited and (b) annealed samples showing relatively aprupt (500Å) interface.

11.5 X-ray diffraction analysis

X-ray diffraction data on as-deposited samples show that both In and In_3Pd were present after deposition. This indicated that In reacted with Pd during evaporation.

Pd/GaAs[6,7] does not form an ohmic contact to n-GaAs. Therefore the results are understood via reactions with In. It is suggested that indium diffuses through the In_3Pd layer to the GaAs interface region forming $In_xGa_{1-x}As$ compounds at the junction which lowers the barrier for electrons, producing an ohmic contact.

A proposed sequence of the reaction is shown in Fig.4. Although the top In layer is molten during the annealing, the In_3Pd layer is expected to remain in the solid state since it has a higher melting temperature ($\approx$ 665°C). Therefore any diffusion process between the In and the GaAs is expected to occur in the solid state. Lattice imaging of the sample indicated that the reacted region is aligned with the GaAs lattice but has a smaller lattice spacing.

Indium reacts with GaAs at low temperatures to form (In-Ga)As alloy compounds, where indium and gallium occupy the same lattice sites. Data from one particular study, shown in the Fig. 6, illustrates the types of compounds formed as a function of anneal temperature. At a given temperature, two distinct groups of compounds are formed, those that are indium rich ($\approx In_{1-\delta}Ga_{\delta}As$) and those that are Ga rich ($\approx In_{\delta}Ga_{1-\delta}As$). For lower temperature anneals, the stoichiometry of the compounds tends toward the two extremes of compositional range. Each individual crystal[12] has a fixed, uniform, single composition and therefore are not graded.

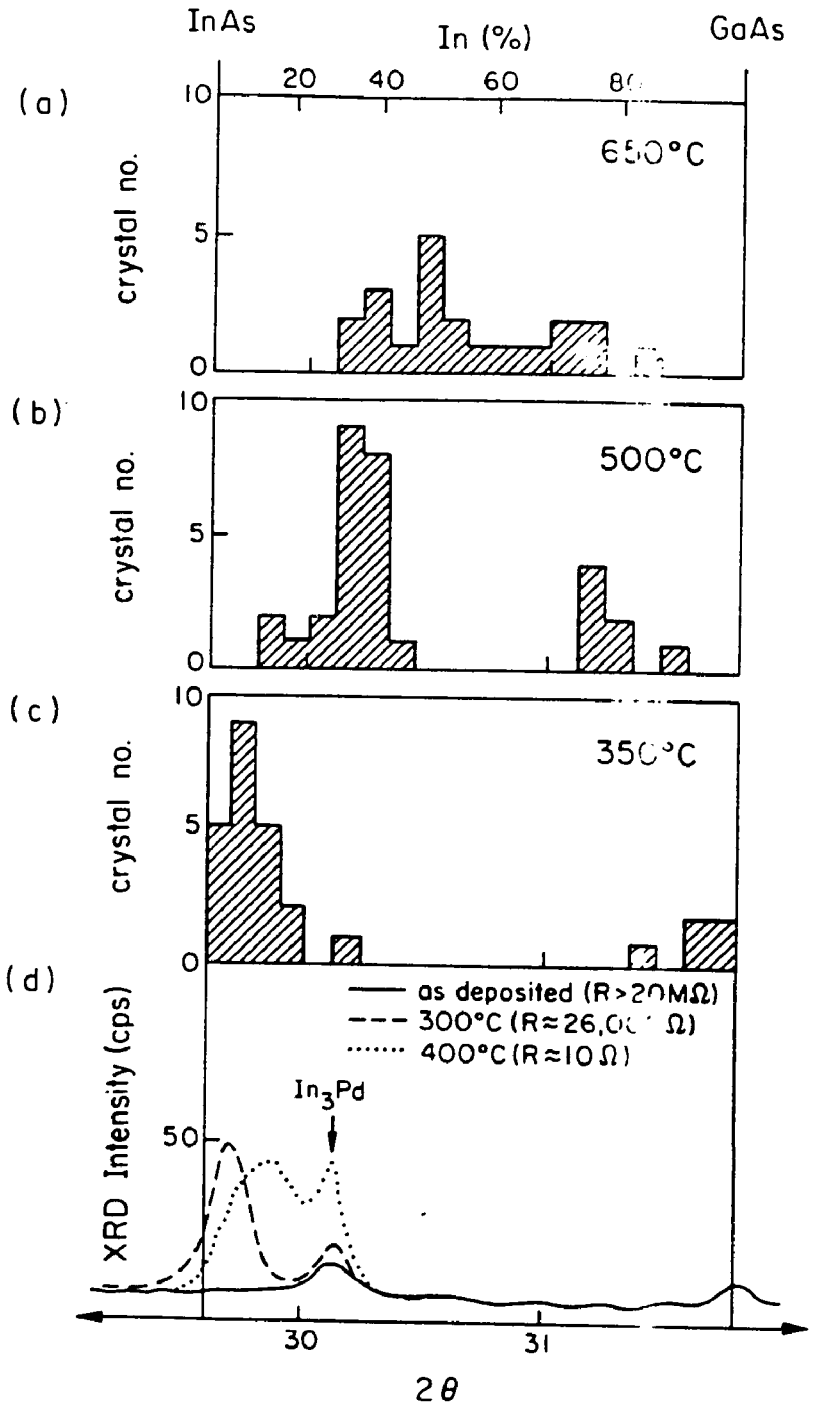


Figure 11.6 Distribution (a-c) of various compositions of $In_xGa_{1-x}As$ grains for different anneal temperatures (after Ding et al[12]) of a sample of 57 nm In on GaAs. X-ray data of (In 4000 Å)/(Pd 400 Å)/GaAs samples annealed at different temperatures is shown in (d) with associated the contact resistance, note the $In_xGa_{1-x}As$ peak relating the value x to 2θ. At low temperatures InAs is formed but at higher temperatures the peak shift indicates that In rich $In_xGa_{1-x}As$ are formed.

In order to identify these alloy compounds, x-ray diffraction (diffractometer) was used. There were three main problems encountered in obtaining the data. First, the peaks were extremely small, on the order of 10 cps (counts per sec) which required long scan times. Second, because the d spacing of the alloy compounds is naturally close to that of the substrate , the alloy peaks are not easily resolved from the large signal of the substrate. And finally, the alloy crystals are strongly oriented with the substrate, the peaks only appear when close to zero tilt so subsequently the sample orientation is of critical importance.

Nonetheless, two low intensity diffraction peaks were observed in the region of the spectrum between the InAs and GaAs peaks, one near the (200) GaAs peak and the other near the (400) GaAs peak. These peaks are attributed to intermediate $In_xGa_{1-x}As$ compounds since the d spacing is linearly related to composition parameter x. To gain more detail regarding the relationship between electrical and material characteristics of the reaction, samples were annealed at different temperatures and then characterized with both electrical and diffraction techniques. Diffraction data is collected with the sample a few degrees off the [100] axis in order do reduce the large diffraction peaks produced by the substrate. In order to avoid redundancy, only the diffraction data near the [200] peak will be presented in this work.

For the as deposited sample the contact resistance is large (>20MΩ) and, as expected, the diffraction peak of the alloy was not observed (Fig. 6). The only peak observed in the region is due to the In_3Pd layer which is present in all samples (even those unannealed) because In and Pd react at room temperature. After (RTA) annealing for 20s at 300°C a diffraction peak of the alloy is observed and has composition very near to InAs. The

resistance of this annealed sample is lowered from >20 MΩ to 26 KΩ as compared to the unannealed sample. Samples annealed for 20 s at 400°C show an even broader diffraction peak extending from the InAs composition toward the intermediate compounds which have a stoichiometry which is richer in Ga concentration. At this temperature anneal (400°C) the contacts show ohmic behavior with a contact resistance of less than 10Ω. This low resistance contact is speculated to be due to a reduction of barrier heights at the interface between intermediate $In_xGa_{1-x}As$ compounds and the GaAs substrate.

Gallium rich compounds of composition near GaAs were not observed in the study, but this is not to claim they were not present. The problem of observing these crystals, if they do exit, may be related to their orientation with respect to the substrate. This topic of preferred orientation is now addressed

To analyze the degree of (epitaxy) orientation between the GaAs substrate and the $In_xGa_{1-x}As$ compounds the samples were first characterized using RBS channelling measurements . These measurements, on 500Å In/ 50ÅPd, did not show significant amount of channelling as shown in Fig.7. This result was also supported with diffraction data shown in Fig.7. X-ray rocking curves of the (200) peak of the alloy crystals indicate that these crystals do have a strong preferred orientation with respect to the GaAs substrate. However, the tilt angle over which the $In_xGa_{1-x}As$ crystals diffract (FWHM ≈ 4°) is wide compared to the rocking curve of the GaAs substrate (FWHM ≈0.5°). The 2θ spectrum of the (200) peak of an annealed sample is shown in Fig.7 for various tilt angles and shows the sensitivity of the $In_xGa_{1-x}As$ peak to tilt angle. It also shows the insensitivity of the In_3Pd peak intensity to tilt angle, which indicates that

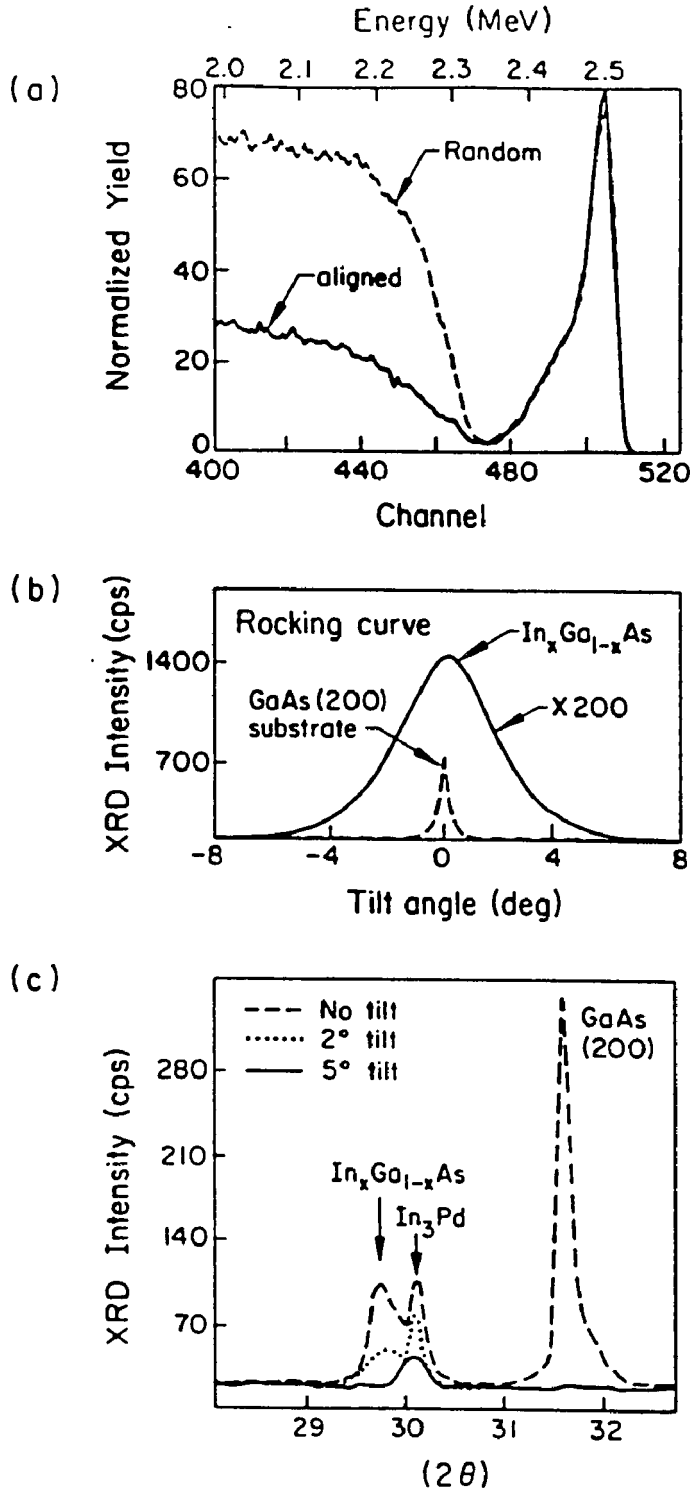


Figure 11.7 (a) RBS spectra of channeling experiment showing little if any alignment of In compounds with the GaAs substrate, and (b) x-ray rocking curves of the (200) $In_xGa_{1-x}As$ compounds and substrate showing strongly preferred orientaion yet not epitaxial alignment of compounds and substrate and (c) a 2θ spectra showing the sensitivity of the In_3Pd, GaAs and $In_xGa_{1-x}As$ peaks as a function of sample tilt.

the In_3Pd crystals are more randomly oriented.

It is expected that the Ga rich alloys compounds (which were not observed) would be even more closely aligned with the substrate and their diffraction peak would be in close proximity to the substrate peak. Together these conditions it would be difficult to resolve the alloy peak from the substrate peak. A better diffraction tool for this application is the double diffractometer.

11.5 Conclusions

Low resistance ($\approx 10^{-6}$ Ω-cm^2) contacts to *n*-GaAs were formed using conventional deposition techniques with In/Pd/GaAs metallization. These contacts were stable under a thermal stress test of 1 hr. at 400°C. The role of the Pd is twofold. It possibly "cleans" the native oxide on the GaAs sample allowing a more uniform reaction between the In and GaAs. It also reacts with the In to form a stable solid state compound (In_3Pd) at the interface and thus provides a buffer zone between the molten In and the GaAs, allowing the In to react with the GaAs in a solid state reaction. The metal GaAs interface is relatively abrupt and shallow having a depth on the order of 500-1000Å.

The intermediate compounds $In_xGa_{1-x}As$ are most likely responsible for the ohmicity of the contact. Only In rich $In_xGa_{1-x}As$ compounds were experimentally identified but others may be present. These crystals had a strong alignment with respect to orientation of the underlying GaAs substrate. Preliminary RBS channelling results indicate that the crystals were not epitaxial with the substrate.

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Chapter 12

Summary and Future Work

The work, presented in Part I of the thesis, can be summarized as a study of crystal growth in an unstable eutectic system. One of the "new" ideas developed here, is that the crystals originate from growth rather than nucleation. This idea is supported by indirect reasoning. The second "new" evaluation is the analysis of the kinetics of the reaction. Due mainly to the simplicity (luck) of the reaction, it is possible to describe the total process in terms of two, more basic, decoupled processes, one related to the number of crystals and the other to the rate of growth. This leads to the relation regarding the activation energies: $E_t = E_v + 1/2\, E_N$. The analysis of the parameter E_N and E_v which are related to more basic parameters of diffusion and of Si-Si bonding is based on models as well as data, so however enlightening the results may be, it still is an indirect evaluation and therefore suspect to later revision.

Future work on this subject branches into four areas. The first area is the continued study of metal-polysilicon reactions from a reliability standpoint. The spiking of PtSi into doped polysilicon is an important problem. It seems possible that the same driving forces, responsible for the Au/polysilicon reaction, could also be involved in the PtSi problem.

The second area is the topic of solid state crystallization. The first thing that should be done is to experimentally measure the diffusivity and solubility of Si in Au. Also, crystals should be grown using the epitaxial

seeding technique and the simplest type device should be fabricated on them, in order to evaluate their electrical characteristics. SOI structures should also be made, then electrically evaluated.

In the third area, it suggested that the field-emitting cathodes be made from the pyramids. At least, the pyramids should be analysed with the TEM. The tips could be looked at without making cross sections.

The fourth area involves growing a crystals from a matrix of SiGe thin films. Au forms another deep eutectic with Ge. Can a SiGe compound be grown heteroepitaxially to a Si or Ge substrate? Does the same phenomena occur in the Au/polygermanium system? One could take this general concept to the ultimate obsession, can diamond be grown using a metal/carbon eutectic system?

The contact resistance chapters of Part II can be summarized as follows. A new technique and analysis method for contact resistance of circular vias has been developed. This system should be tested over a greater range of via diameters, perhaps with the new photomask set currently in use at IBM.

Selective W deposition on Al has proven to be a difficult process. The results are probably very machine-dependent. However, a machine which has the capability for *in-situ* sputter-cleaning should make a formidable contribution to process control.

And finally, comments are now made on the GaAs study. Ohmic contacts using In/Pd metallization were successfully made. Analysis indicated that InGaAs compounds are formed during thermal anneal. Preliminary results show that these contacts are shallow, less than a 1000 Å deep. Real devices should be made with these type contacts to show if they do provide any advantage in devices which require shallow ohmic contacts.

Appendix A

Here we model the region near the growing crystal, relating the dissolution rate (B) of the polysilcon and the diffusion coefficient of Si in Au (D) with the relative concentration (C) of Si in Au at a position (r) relative to the crystal position. It is assumed that the crystals have reached a steady-state rate of growth and that the size of the crystals is much less than the distance between the crystals.

Assume that the flux of Si, $J_z(r)$, dissolving from the polysilicon is linearly dependent on the deviation of the local Si concentration C(r), we obtain the relation

$$J_z = B\,[\,C_o - C\,]\ , \qquad \text{(A1)}$$

where C_o is the concentration far away from the crystal. The continuity equation

$$I'(r) = 2\pi r\, J_z \qquad \text{(A2)}$$

relates the total flux of Si I(r) to the local Si flux from the polysilicon, where $dI/dr = I'(r)$. Using Fick's first law

$$J_r = -D\,C'\ , \qquad \text{(A3)}$$

and the relation $I = d_{Au} 2\pi r\, J_r$, where d_{Au} is the gold thickness, we obtain the differential equation

$$C'' + C'/r - C/L^2 = -C_o/L^2\ . \qquad \text{(A4)}$$

The solution to this equation is a modified hyperbolic Bessel function $K_o(x/L)$ where $L^2 = d_{Au} D/B$, and C_0 is the Si concentration at the crystal edge r_o. The factor L (μm) can be interpreted as an effective diffusion length. A plot of the Si concentration and fluxes for this model are given in Fig. 4.10.

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