Predictive Simulation of ESD-induced Failures in Microelectronic Systems

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System-level ESD Reliability

• Currently achieved with a combination of
  o Expert know-how
  o Trial-and-error design modifications when a product fails qualification testing or a customer complains

• Better alternative: use simulation to verify product ESD robustness during the design phase
  o Prior to manufacturing
  o This approach is advocated in JEDEC Publication 161

• Why isn’t this the default approach?
  o Simulation challenges: feature sizes range from cm to nm
  o Modeling challenges: component suppliers don’t provide models of the ESD response
Attack the Challenge

- Predictive simulation of system-level ESD simulation is a very big challenge. How to tackle it?
  - Be less ambitious: Predict hard failure only
    - E.g., SEED methodology proposed by the Industry Council on ESD Target Levels
    - Hard failure is relatively easy to simulate, since it usually results from contact discharge to a signal trace, which is amenable to circuit-level simulation
      - ML can improve the model accuracy
  - Be very ambitious—hard and soft failures, contact and air discharges
    - Use machine learning to address the modeling challenges
System-efficient ESD Design (SEED)

Figures from JEP-161
Simulation Netlist

- ESD source (e.g., gun), connector, trace, on-board protection (e.g., TVS), signal line filter, IC
- Component vendor may provide an IBIS model but ESD-relevant model is needed
- Industry Council suggests that the ESD model be fit to the (high-current) pulsed I-V characteristic
  - E.g., piece-wise linear function
  - Customer can generate model if not provided by supplier

Figures: S. Bertonnaud et al., 2012 EOS/ESD Symp.
Shortcomings of Static I-V Models

- Ignores turn-on transient; over-voltage stress is most severe during this interval
  - Industry Council suggests: run 2 sets of sims using I-V models for long and short pulsewidth
  - However, I-V curve may have additional shifts in time due to time-out of on-chip protection
    - A bona-fide transient model would address these issues → must be an efficient, behavioral model
- I-V curve at the signal pin is not a fixed property of the component; it is affected by the board PDN
  - Need multi-port models or PDN-aware models
    - ML methods used to quickly generate such models
Improved I-V Models

Non-parametric regression (kernels, splines) used to learn

\[ V_{10} = f(I_{ESD}, \tau_{pw}, board \ PDN) \]

J. Xiong, UIUC/CAEML
Transient Behavioral Model

Verilog-A RNN Model

Z. Chen, UIUC/CAEML
Transient Model Discussion

- Transient models improve simulation accuracy
- Challenge: high-quality training samples
  - Generate using circuit simulation
    - Need complete netlist – designer yes; customer no
    - Need ESD compact models, not regular PDK models
  - Measurement data
    - Need to measure the component response to a variety of high-amplitude stimuli
    - Ordinary TLP tester is inadequate
      » Produces 100-ns pulses with 10-ns rise-time
Stochastic Modeling of Soft Failures

• As-yet unpublished material removed …