

CAEML BULLETIN

DIRECTOR'S LETTER

I want to use this opportunity to welcome CAEML's newest industry member, Synopsys. Let me also give a special shout-out to Chris Cheng of HPE, who suggested I be invited to give a keynote lecture at DesignCon 2017. My talk there covered machine learning and its application to EDA; you may download a copy of my presentation slides (missing the animation and embedded video) from the CAEML website, go.illinois.edu/caeml. The three CAEML site directors - Paul, Madhavan and myself - appreciate all the aid the IAB provides in regards to corporate outreach and new member recruitment.



Research projects commenced in January, at the start of the Spring semester. We look forward to sharing our early results with you at the IAB's semiannual meeting on April 25-26. If you have not yet made travel arrangements, please do so. Recall that a member company may choose to send more than one person to the semiannual meeting, and we would welcome the additional technical interactions. However, all attendees must pre-register; a link to the registration page is available on the CAEML website under EVENTS at http://go.csl.illinois.edu/Spring_2017_IAB_Meeting.

We look forward to seeing you all at Georgia Tech in Atlanta.
Elyse Rosenbaum

PROJECT UPDATES

Modular Machine Learning for Behavioral Modeling of Microelectronic Circuits and Systems: Lead Investigator Maxim Raginsky (Co-PI Andreas Cingellaris)

In the two months since this project was initiated, we have made progress in the following directions:

- Local and global stability analysis of gradient descent with back propagation.
- Composability of learned recurrent neural network models with circuit simulators (in collaboration with Zaichen Chen and Professor Elyse Rosenbaum).

- Integrating flexible generative models into a passive macromodeling pipeline (with Xiao Ma and Professor Andreas Cingellaris).

Intellectual Property Reuse through Machine Learning: Lead Investigator Paul Franzon (Co-PI Brian Floyd)

The goal of this project is to develop a machine learning-based flow that permits design analysis, design optimization, and Intellectual Property reuse of analog circuit blocks.

We have developed a flow that has two steps: design analysis and design optimization. IP reuse is achieved by optimizing the same analog topology in the target node.

We have successfully applied this flow to optimize and reuse two tape-out quality 77-GHz analog blocks, including a balun and a power amplifier. Results show that our proposed flow leads to better design than does a human designer and also significantly outperforms evolutionary algorithm-based simulator-in-loop approaches in terms of total simulation sample consumptions. (Graduate Students: Weiyi Qi, Weihu Wang, and Yi Yang)

Design Rule Checking with Deep Networks: Lead Investigator Paul Franzon (Co-PI Rhett Davis)

Researchers at NCSU have started this project by focusing on automating tool flow setup for the Xilinx place and route (P&R) tools. To date, the effort has focused on tool and environment setup. We plan to instrument these flows so they can be automatically conducted and measured in the SUMO environment. (Graduate Student: Billy Huggins)

Behavioral Model Development for High-Speed Links: Lead Investigator Madhavan Swaminathan (Co-PIs Jose Schutt-Aine and Paul Franzon)

The research team's recent efforts included the following:

- Artificial neural networks (ANN) for developing behavioral models of oscillators. Frequency-based training is being used to generate periodic output waveforms. Preliminary results are very promising and can be adapted to oscillators with controls. (Graduate Student: Huan Yu; Visiting UG Student: Rajath Raguraman)

- Polyharmonic distortion (PHD) based modeling of electronic systems that include nonlinearities. The relationship between incident and scattered waves is described using not only port-to-port but also harmonic-to-harmonic interactions. (Graduate Student: Thong Nguyen)
- System identification was used to produce models that include noise impact (such as Power Supply Induced Jitter) on high-data rate receivers. Training data included measurements and a 32 nm reference design. (Graduate Student: Bowen Li)

- We are working on the use of Multi-Layer Perceptron (MLP) neural networks and Gaussian Processes as surrogate functions for adaptively generating data samples for constructing high dimensional black box models and for design optimization. (Graduate Student: Hakki Mert Torun)

[1] S. J. Park, B. Bae, J. Kim and M. Swaminathan, "Application of machine learning for optimization of 3-D integrated circuits and systems," *IEEE Trans. VLSI*, 2017.

Models to Enable System-level Electrostatic Discharge Analysis: Lead Investigator Elyse Rosenbaum

During the project's first two months, the research team's efforts were focused on the following tasks.

- Collection of training data using both simulation and measurement. For the latter, two new measurement systems were developed. One of these is an automated, speed-controlled system for air discharge testing that has been incorporated into an IEC 61000-4-2 standard testbed.
- Investigation of recurrent neural networks (RNN) for ESD modeling of nonlinear components (ICs). A novel regularization scheme was developed to ensure that the learned model is stable, and a method to obtain a continuous-time approximation of the RNN for implementation in Verilog-A was developed. This task was done in collaboration with Prof. Max Raginsky.

(Graduate Students: Zaichen Chen, Sam Sagan, and Jie Xiong.)

Optimization of Power Delivery Networks for Maximizing Signal Integrity: Lead Investigator Madhavan Swaminathan (Co-PI Chuanyi Ji)

The research team is exploring the use of Bayesian optimization for power grid optimization, leveraging the teams' recent work where 38% improvement in CPU time was achieved compared to other optimization techniques when applied to 3D systems [1]. Other activities undertaken at the project start include the following:

- We have been investigating techniques that will improve upon Monte Carlo and polynomial chaos-based methods for stochastic modeling. The team is working on support vector machines, neural networks, and variational auto-encoders. (Graduate Student: Majid Ahadi)

Student Spotlight



Weiyi Qi is a Ph.D. student in the Department of Electrical and Computer Engineering at North Carolina State University. He joined Dr. Paul Franzon's research group in 2012. Weiyi's research focuses on machine learning-enabled EDA methodology, including circuit/system performance optimization via statistical learning and predictive modeling for computationally expensive and high-dimensional designs. He currently leads the analog IP reuse project in the CAEML center and will graduate in summer 2017.

Weiyi is from China and graduated in 2011 from Dalian Jiaotong University with a B.S degree in Electronics and Information Engineering. He went on to earn an M.S degree from North Carolina State University in 2013. His plan after graduation is to seek a position in industry.